Extended Abstracts of the 2017 International Conference on Solid State Devices and Materials, Sendai, 2017, pp185-186

Read Disturb Improvement for 1znm TLC NAND Flash

Ho-Nam Yoo, Hyunyoung Shim, Jong-Wook Kim, Keum-Hwan Noh, Heehyun Chang

Flash Development Division, SK Hynix Inc.
337 Jikji-daero(Bldv), Hyangjeong-dong, Hungduk-gu, Cheongju-si, 361-725, Republic of Korea
Phone: +82-43-280-3151 E-mail: honam.yoo@sk.com

Abstract

The read disturb is one of main problem of NAND flash memory reliability. As NAND flash memory is scaled down, read disturb is degraded because tunnel oxide is thinner and read number is increased due to increased WL string number. Especially read disturb is worse in TLC than MLC, because of higher read pass bias (VpassR). We carefully investigated FN tunneling phenomena at various electric field range and we found read disturb is occurred by low field FN tunneling. Therefore, we optimized doping profile of floating gate to minimize low field FN tunneling. As a result, we successfully achieved good read disturb characteristics compared with previous tech NAND flash.

1. Introduction

As the density of NAND flash memory increases using advanced process techniques such as shrinking process and multi leveling, the read disturb problem is expected to emerge as a major reliability concern for future high-density NAND flash memory [1]. Read Disturb errors are an intrinsic result of the flash architecture [2]. In NAND flash, data is stored as the threshold voltage of each cell, which is based on the logical value that the cell represents. During a read operation, a read reference voltage is applied to control gate of selected cell. Within a NAND flash block, the transistors of multiple cell has a same bit line. Only one cell is selected at a read operation. Therefore, in order to read one cell, the unselected transistors must be turned on to pass through the value of selected cell read. The pass through voltage (Vpass) should be higher than any threshold voltage of unselected cells. Though these unselected cells are not read, high pass through voltage induces electric tunneling that can shift the threshold voltage to higher values. As we scale down the size of NAND flash cells, the transistor oxide becomes thinner which increases tunneling effect (by Fowler-Nordheim tunneling). As a result, read disturb is deteriorated and it takes fewer read numbers for unselected cells to become disturbed and move into a different logical states.

To improve read disturb, we investigated read disturb at the point of FN tunneling.

- Each NAND flash cell has different Fowler-Nordheim (FN) tunneling characteristics because of process variation.
- FN tunneling can be suppressed by changing band structure of floating gate.

In this paper, we improved read disturb of 1znm TLC NAND flash memory by engineering electron band structure of floating gate.

2. General Instructions

NAND Flash Program Operation and Read Disturb

FN tunneling is commonly used for NAND flash cell programing, allowing a high-efficiency electron transfer to floating gate [3]. The memory cells are programmed by FN tunneling of electrons from the inversion layer of substrate to the floating gate when a high voltage is applied to the control gate while the drain and source regions are grounded [4].

The NAND flash cells share one bit line, which is connected to the sense amplifier. In order to read one cell on the bit line, all of the other cells must be switched on. We turn on these unselected cells by applying the pass through voltage which is higher than threshold voltage of unselected cells. This pass through voltage can cause the FN tunneling of unselected cells to a higher threshold voltage. While a single threshold voltage shift is small, such shift can be piled up over time, eventually becoming large enough to alter the logical state of some cells and generate read disturb errors.

FN tunneling characteristics

As we mentioned before, read disturb characteristics has relation with FN tunneling. But in some cells, program characteristics is not correlated with read disturb characteristics, even though both of two phenomena are related with FN tunneling. To analyze this discrepancy between program and read disturb characteristics, we measured the threshold voltage change of two NAND flash chips by programming with various program bias. Figure 1 (a) and (b) show program characteristics of two different samples. Sample A and sample B have same program characteristics in high bias range. On the other hand, sample A shows faster program characteristic than sample B in low bias range, and read disturb characteristics is worse in sample A (Fig.1 (c)). Consequently, high bias program and low bias program characteristics are different in each cell, and read disturb is occurred by low field FN tunneling.

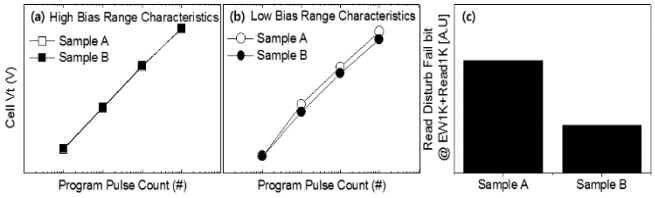

Fig. 1 Program characteristics under various program bias and pulse count, and read disturb characteristics of each sample.

Floating gate doping profile engineering

FN tunneling is occurred at tunnel oxide interface. Therefore, FN tunneling is influenced by band structure of tunnel oxide interface and floating gate. To modulate band structure, we engineered floating gate doping profile which can reduce low field FN current. As shown in Fig. 2, we inserted undoped poly silicon layer into bottom of floating gate for bane engineering. As a result, low field FN current is decreased in optimized floating gate, as shown in Fig. 3.

At low control gate bias, contrary to conventional floating gate, optimized floating gate has depletion layer at the bottom of floating gate (Fig.4). And this depletion layer reduces electric field at dielectric layer. Therefore, low field FN current is decreased and read disturb is improved. But high field FN current, which is involved in conventional program operation, is not changed because depletion layer is not formed at high field in optimized floating gate, which means that conventional program operation is not affected by the change of doping profile. Consequently, as shown in Fig. 5 and Fig. 6, after read stress, erase cell Vt distribution shift is decreased and max fail bit is decreased by 35% in optimized floating gate.

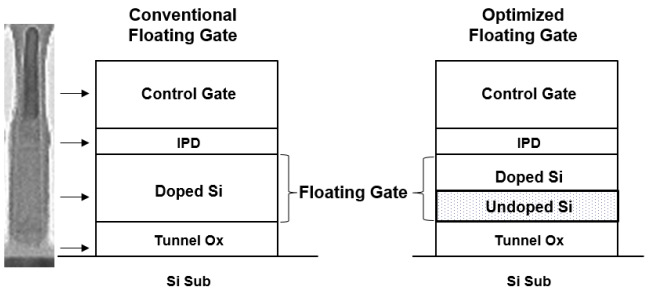

Fig. 2 Schematic structure of conventional floating gate and optimized floating gate.

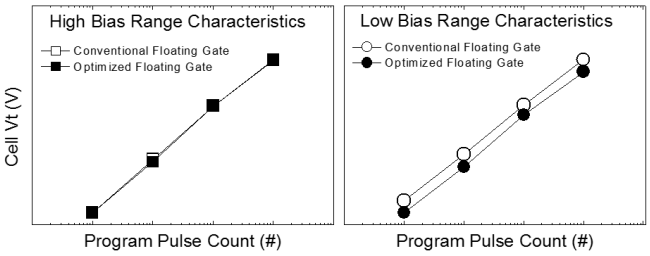

Fig. 3 Program characteristics of optimized floating gate

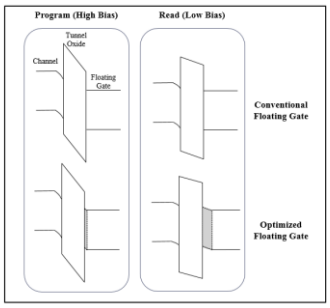

Fig. 4 Band diagram of conventional floating gate and optimized floating gate

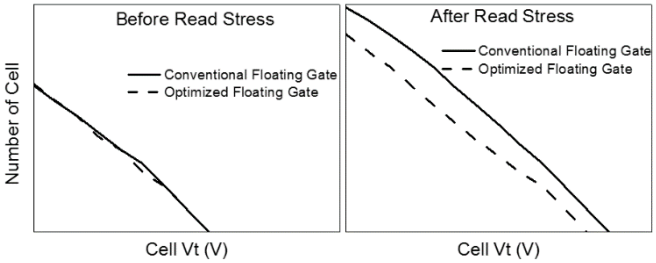

Fig. 5 Erased cell Vt distribution of conventional floating gate and optimized floating gate. Optimized floating gate has smaller shift than conventional floating gate after read stress.

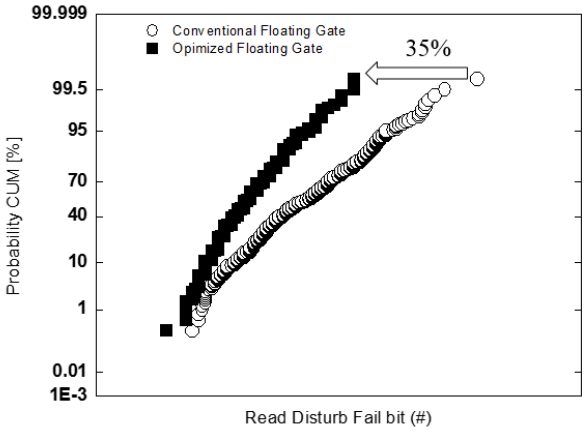

Fig. 6 Optimized floating gate has better read disturb characteristics.

3. Conclusions

We investigated FN tunneling characteristic at various electric field range, and found that read disturb is occurred by low field FN tunneling. Then we engineered floating gate doping profile to minimize low field FN tunneling. As a result, we achieved better read disturb characteristics than previous tech NAND flash.

References

[1] Keonsoo Ha, Jaeyong Jeong, and Jihong Kim, "A Read-Disturb Management Technique for High-Density NAND Flash Memory," in Proceedings of the 4th Asia-Pacific Workshop on Systems, Singapore, 2013. pp. 1-6.

[2] Y. Cai, Y. Luo, S. Ghose, E. F. Haratsch, K. Mai, and O. Mutlu, "Read Disturb Errors in MLC NAND Flash Memory: Characterization, Mitigation, and Recovery," in Proceedings of the 45th annual IEEE/IFIP International Conference on Dependable Systems and Networks (DSN), Rio de Janeiro, Brazil, 2015, pp. 438-449

[3] C. Monzio et al., "Ultimate accuracy for the NAND Flash program algorithm due to the electron injection statistics", IEEE Trans. Electron Devices, vol. 55, Oct. 2008, pp. 2695-2702.

[4] G. J. Hemink, T. Tanaka, T. Endoh, S. Aritome, R. Shirota, "Fast and accurate programming method for multi-level NAND EEPROMs", 1995 Symp. VLSI Tech. Dig., 1995, pp. 129-130.