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Characteristics of Crystalline Oxide Semiconductor-based Single Transistor Multiplier for Analog Neural Network

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Abstract

An analog neural network (ANN) based on a single transistor multiplier (STM) configured with crystalline oxide semiconductor FETs (OS-FETs) is evaluated. The STM retains a multiplier factor in nonvolatile analog memory formed with OS-FET. OS-FETs are fabricated on a glass substrate. Device characteristics of the STM have evaluated and ANN operation is demonstrated.

1. Introduction

Analog implementation of circuits, for example, a multiply-accumulate (MAC) circuit enables operation with a small number of elements compared with a digital implementation of the circuits (Table I). However, it is difficult to obtain practical analog memory in terms of size and accuracy (Table II).

A crystalline oxide semiconductor FET (OS-FET) [1] with ultra-low off-state current (I_{off}) can build nonvolatile analog memory that is capable of storing analog data and has high endurance when used as a switch for a charge retention node. The OS-FET has a wide voltage use range in a saturation region because it has high breakdown voltage owing to a wide bandgap of the OS. Moreover, the increase in mobility of the OS-FET by optimization of OS deposition process has been recently proposed [2]. Therefore, the OS-FET seems to be suitable in analog implementation.

In this work, device characteristics of a single transistor multiplier (STM) combined with analog nonvolatile memory formed with OS-FETs fabricated on a glass substrate are investigated. Moreover, the feasibility of an analog neural network (ANN) using the STM is also confirmed.

2. OS-FET Device Characteristics

The OS-FET fabricated on a glass substrate is adopted in this work. Its cross-sectional view is shown in Fig. 1. Various OS-FET device characteristics are shown in Figs. 2(a) to 2(e). The transfer characteristics, V_{GS}–I_{DS}, in Fig. 2(a), indicate that the OS-FET has excellent switching characteristics with an S value of 120 mV/decade. In addition, the transfer characteristics, V_{GS}–$\sqrt{I_{DS}}$, in Fig. 2(a) and the drain characteristics, V_{DS}–I_{DS}, in Fig. 2(b), show good saturation characteristics in a wide voltage range that is capable of voltage overdrive. Moreover, cutoff frequency is 100 MHz as shown in Fig. 2(c), and the off-state current, I_{off}, estimated from a test element group (TEG) circuit configuration [1] is 10^{-22} A at room temperature as shown in Fig. 2(d). The 1/f noise characteristics are shown in Fig. 2(e). There has been a report that an OS-FET which is fabricated on a glass substrate and transferred to a flexible substrate does not affect device characteristics even it is bent [3]. These features are benefits in applying the OS-FET to analog memory and analog operation in large-area electronics.

3. Single Transistor Multiplier (STM)

Circuit diagrams and micrographs of a STM configured with the OS-FETs and a STM array where STMs are arranged in a matrix are shown in Fig. 3 and Fig. 4, respectively. The STM has a 2T1C configuration. Specifications of the fabricated STM array chip are shown in Table III. M1 controls storage of analog data to a charge retention node FN. The node FN is regarded as a nonvolatile storage node because the OS-FET exhibits ultralow I_{off}. If the STM is applied to a multiply operator in the NN, the node FN corresponds to analog memory for retaining a learned weight-factor W. The voltage V_{FN} of the node FN varies through a 100-fF capacitor C1 in response to input data supplied to X; thus, the amount of drain current of M2 changes. Current corresponding to the multiplication value of X and W can be extracted from the drain current by appropriate operation such as subtraction of offset current according to the formula [4]. Furthermore, an analog MAC unit is achieved by summing up currents of STMs; therefore, it can be built in each column of the STM array.

Transfer characteristics of the STM ($X \times W$) calculated based on the amount of drain current in M2 that is obtained by scanning X for each W are shown in Fig. 5(a). As shown in Figs. 5(a) and (b), multiplication with 5-bit accuracy is performed in a voltage range of 4 V and at center bias of $X = 8$ V. Frequency response of the STM is shown in Fig. 5(c), where the maximum frequency is approximately 10 kHz, which is limited by the parasitic capacitance of an output pad of the fabricated TEG. SPICE simulation results indicate that the frequency response is approximately 1 MHz when the parasitic capacitance is changed to 0.1 pF. The total harmonic distortion (THD) is shown in Fig. 5(d). The THD at 1 kHz is more than 25 dB. When the analog memory configured with OS-FETs whose I_{off} is 10^{-22} A is used with 5-bit accuracy and a voltage range of 4 V, a charge retention time is estimated to be approximately 8.1 years.

4. Analog Neural Network with STM

The analog MAC units can be built in the STM array to realize ultra-parallel operation; thus, a convolutional NN (CNN) is promising as a good application of the STM array. In order to confirm that the STM array can be used in the CNN for pattern recognition, a four-layer ANN system shown in Fig. 6(a) is built to perform learning and recognition of handwritten characters using MNIST as a learning data set. In this system, the rate of correct recognition for test images of MNIST is calculated for various operation accuracies. The ANN system is confirmed to correctly recognize handwritten characters at the rate of 99.02% with the operation accuracy of 5-bit as shown in Fig. 6(b); thus, the accuracy of the STM (5-bit) is high enough to perform the recognition. The power consumption of the STM array is 512 μW when 16 (4×4) multiplications are performed in parallel. When the STM array operates at 1 MHz, operation efficiency is estimated as high as 31 GOp/s/W, which is higher than that of a

conventional high-performance computer [5].

5. Conclusions

An ANN based on STMs configured with OS-FETs has been proposed. The demonstration results show the ANN scores better operation efficiency than the conventional digital computers and the OS-FET is suitable for analog implementation.

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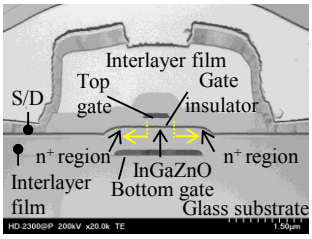

Fig. 1 TEM image of OS-FET on a glass substrate

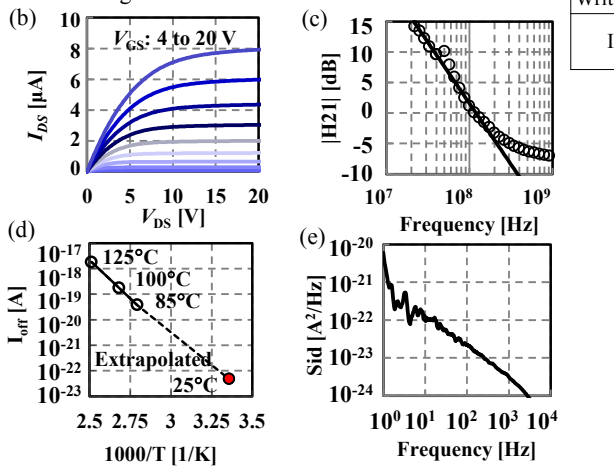

Fig. 2 OS-FET characteristics (L/W = 10 μm/10 μm)
(a) Transfer characteristics (b) Drain characteristics
(c) Frequency response (d) Off state current (e) 1/f noise characteristics.

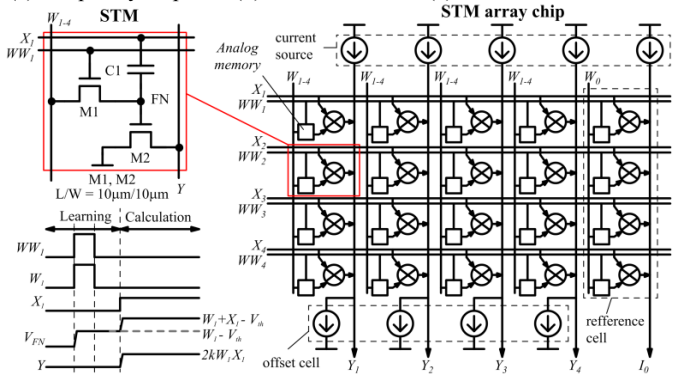

Fig. 3 Circuit configuration of STM and STM array.

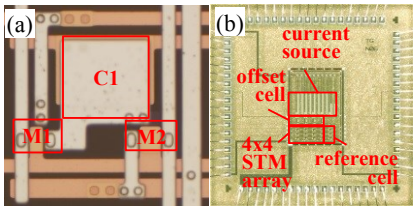

Fig. 4 Micrographs of (a) STM (b) STM array chip.

Table III STM Array Chip Specifications

STM size	100 μm sq.
Technology	3 μm
Supply voltage	16 V
# of STM	4 × 4
Chip size	5 mm sq.

Table I Comparison among Multipliers

	This work	Trans-conductor [6]	Gilbert [7]	Switched capacitor matrix [8]
Circuit	2 T + 1 C	8 T	10 T	More than 10 T + C
Accuracy	5 bits	7 bits	8 bits	6 bits

Table II Comparison among Analog Memory

	OS-FET [3]	MRAM [9]	ReRAM [10] PCM [11]	Flash memory [12]	Switched capacitor [13]
Accuracy	8 bits	6 bits	3 bits	4 bits	>8 bits
Writing cycle	>10^{13}	10^{16}	10^{12}	10^{5}	Unlimited
Issues		2-terminal Small range	2-terminal Large degradation	Endurance	Large size

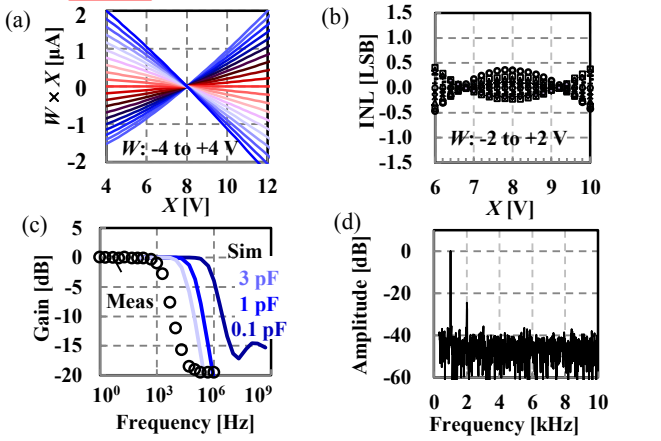

Fig. 5 STM characteristics (a) Transfer characteristics
(b) Integral Nonlinearity (INL) converted into 5-bit accuracy
(c) Frequency response (d) Total harmonic distortion at 1 kHz.

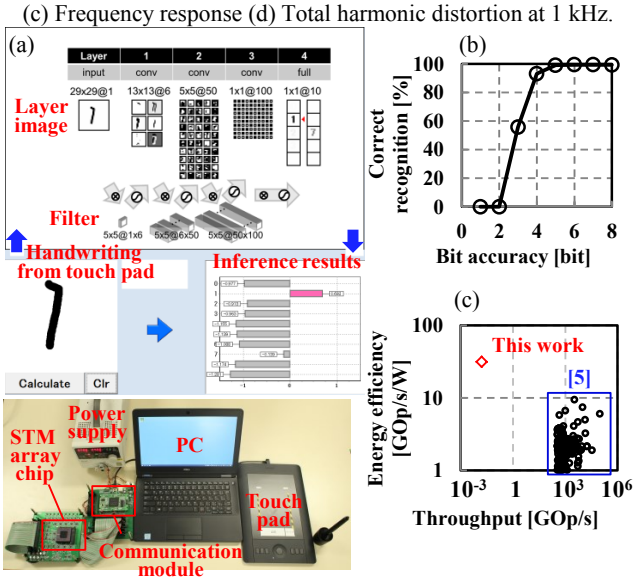

Fig. 6 (a) ANN system (b) bit accuracy dependencies on the rate of correct recognition (c) Energy efficiency of STM array