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Improved Performance and Sufficient Reliability $In_{0.53}Ga_{0.47}As$ FinFET Using NH_3 Plasma Treatment

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Abstract

We present the $In_{0.53}Ga_{0.47}As$ FinFET utilizing NH_3 passivation effects in a post remote plasma (PRP) process. A good immunity to the short channel effects is achieved and the performance is greatly improved with the high fin aspect ratio (H_{FIN}/W_{FIN}). Device with L_{CH} = 50 nm, W_{FIN} = 20 nm, and H_{FIN} = 50 nm exhibits $I_{on}/I_{off} \sim 10^5$, I_{DS} = 1600 μA/μm (V_{GS} - V_{TH} = 1 V), and $G_{m,max}$ = 2282 μS/μm (V_{DS} = 0.5 V). Besides, the positive bias temperature instability (PBTI) measurements indicate that the plasma-treated InGaAs FinFETs are quite reliable with a small threshold voltage shift and a long-term operation.

1. Introduction

Recently, high aspect ratio (AR) 3D III-V MOSFETs such as FinFET or nanowire/GAA FET have been considered as the promising structures to drive the CMOS technologies into sub-nanometer region [1], [2]. However, the etching-process-induced damage at the sidewall/surface of nano-patterned III-V structures needs to be addressed as one of the sources of performance degradation. In addition, the inherently poor quality of high-k/III-V interface has not been satisfied, contributing to the deterioration of III-V device characteristics. In this work, we propose NH_3 interfacial treatment in a post remote plasma (PRP) process to demonstrate the improved electrical performances InGaAs FinFET follow the fin ARs. From the PBTI reliability studies, the InGaAs FinFET treated by PRP treatment, being beneficial for passivating or recovering the sidewall of high-k/III-V FinFET, provides stable material properties for long-term operation.

2. Experimental Procedure

The epitaxial structure used in this study consisted of 50 nm p-$In_{0.53}Ga_{0.47}As$ (5 x 10^{16} Be doped) channel layer and 100 nm p^+-InP buffer layer on the p^{++}-InP substrate grown by solid source molecular beam method as the starting material. After surface degrease, 10 nm Al_2O_3 was grown by atomic layer deposition (ALD) as a dummy layer. Source/drain Si implantation was then performed and the dopant activation was carried out by rapid thermal annealing (RTA) in a nitrogen ambient. Then, the fin was defined via electron-beam lithography. The fin profile was done by inductively coupled plasma (ICP) dry etching and citric acid as a wet etching process. Next, the gate oxide was deposited after chemical pre-treatment with HCl (1:10) and $(NH_4)_2S$. In ALD chamber, 5 nm Al_2O_3 was applied as gate oxide followed by in situ PRP treatment using NH_3/N_2 gases with a plasma power of 150 W for 2 minutes. Some FinFET devices were fabricated without any in situ PRP treatment as the control samples. Finally, TiN gate metal, Au/Ge/Ni/Au S/D ohmic, and AuBe backside contact were formed and finished by post metallization annealing at 300°C in N_2 for 30 seconds. Fig. 1 shows the TEM images of a completed device featuring the fin profile with 20 nm fin width and 50 nm fin height.

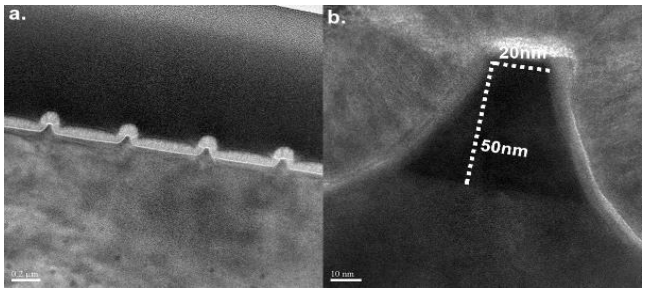

Fig. 1 TEM of completed device (a) fins across the gate pattern and (b) the fin dimension with 20 nm fin width and 50 nm fin height.

3. Results and Discussion

Fig. 2(a) and (b) show the output characteristics and transconductance ($G_{m,max}$) of fabricated InGaAs FinFETs with channel length (L_{CH}) of 80 nm, fin width (W_{FIN}) of 50 nm, and fin height of (H_{FIN}) of 50 nm for samples with and without PRP treatment. As compared to the control sample, the I_{DS} and $G_{m,max}$ increased 2.25 times and 3 times, respectively, for PRP treated sample. Significant improvements were clearly observed which can be attributed to the nitrogen-passivation effects obtained by the plasma process. Fig. 2(c) and (d) show the transfer and output characteristics of an L_{CH} = 50 nm, W_{FIN} = 20 nm, and H_{FIN} = 50 nm FinFET treated by PRP. This

device shows normalized I_{DS} of 1600 μA/μm at $V_{GS} - V_{TH}$ = 1 V and V_{DS} = 1 V, $G_{m,max}$ of 2282 μS/μm, subthreshold swing (SS) of 100 mV/dec at V_{DS} = 0.5 V, drain induced barrier lowering (DIBL) of 80 mV/V.

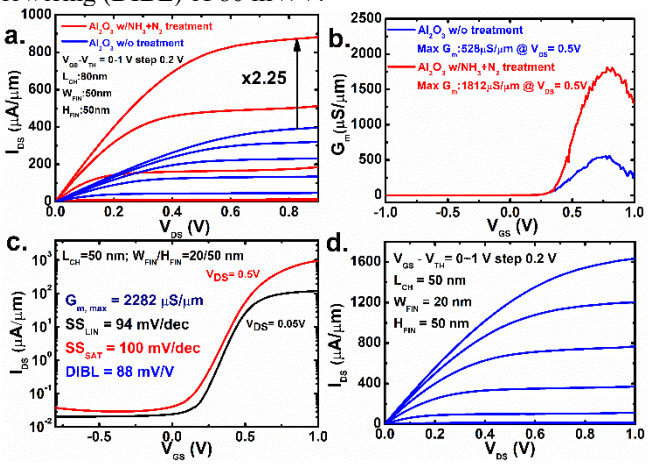

Fig 2. (a) Output and (b) transfer characteristics for InGaAs FinFETs with and without PRP treatment. (c) and (d) The electrical properties of an InGaAs FinFET with L_{CH}=50nm, W_{FIN}=20nm, H_{FIN}=50nm.

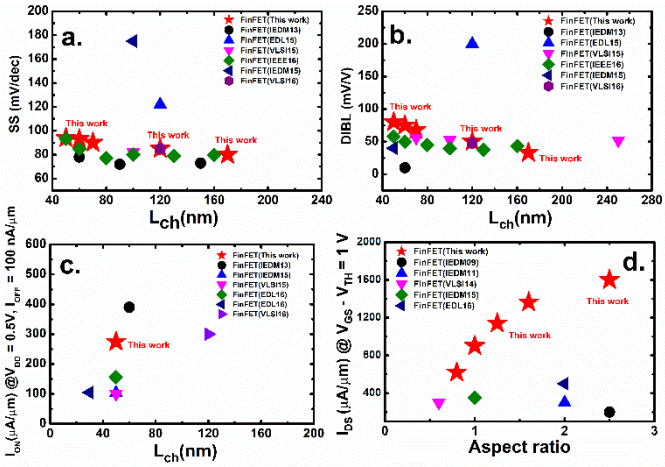

Fig 3. The devices benchmarked against the state-of-the-art InGaAs FinFETs. (a) SS, (b) DIBL, and (c) I_{on} at V_{DD}=0.5V&I_{off}=100nA/μm versus L_{CH}; (d) I_{DS} at V_{GS}-V_{TH}=1V versus aspect ratio.

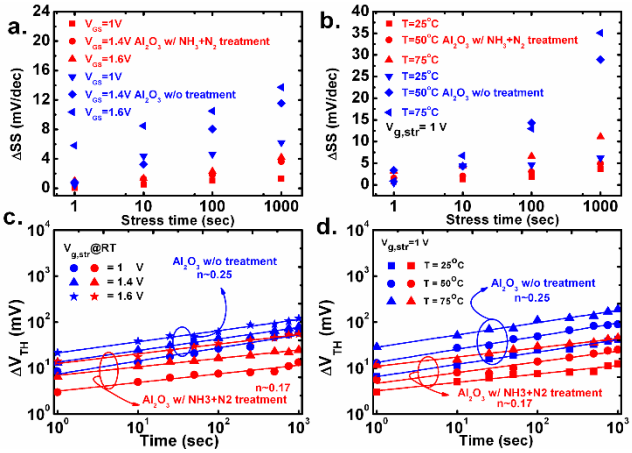

Fig 4. Time evolution of (a), (b) subthreshold swing degradation (ΔSS) and (c), (d) threshold voltage shift (ΔV_{TH}) under PBTI stress for InGaAs FinFETs with and without PRP treatment.

Fig. 3 benchmarks the electrical characteristics of InGaAs FinFET presented here against those published to date [3-13]. Our results show excellent gate control ability which related to the improved performance of the scaled devices with high fin AR. This also proves that passivation the interface states at the sidewall of the high AR FinFETs play an important role in providing better electrostatic control.

Fig. 4 plots the time evolutions of the subthreshold swing degradation, ΔSS, (Fig. 4(a) and (b)) and the threshold voltage shift, ΔV_{TH}, (Fig. 4(c) and (d)) under PBTI stress for different stress voltages, $V_{g,str}$, and temperatures, T, for the InGaAs FinFETs with and without PRP treatment, respectively. For the PRP treated samples, both ΔSS and ΔV_{TH} against stress time follow the power law relation. A lower time exponent (*n*) value observed here indicates lower trap generation and electron trapping rates under different stress conditions, associated with a better PBTI reliability lifetime.

3. Conclusions

In this work, we illustrated the improved performance and reliability on the $In_{0.53}Ga_{0.47}As$ FinFETs using post remote plasma treatment. The device shows $I_{on}/I_{off} \sim 10^5$, I_{DS} = 1600 μA/μm (V_{GS} - V_{TH} = 1 V), SS = 100 mV/dec and $G_{m,max}$ = 2282 μS/μm (V_{DS} = 0.5 V). In addition, from the PBTI reliability studies, the FinFETs treated by PRP treatment were observed to exhibit stable material properties after long-term operation.

Acknowledgements

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