Single and Double Diffusion Breaks in 14nm FinFET and Beyond

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Abstract
Layout-dependent effect (LDE) in FinFET technology is investigated by means of TCAD process and Monte-Carlo device simulation. A good agreement is obtained when comparing to experimental data on 14nm FinFET with double diffusion break (DDB). Single diffusion break (SDB) in 7nm FinFET is discussed. Simulation indicates that stress relaxation is pronounced in case of DDB and self-aligned SDB, while non-self-aligned SDB preserves stress at the price of high variability.

1. Introduction
The layout-dependent effect (LDE) on stress and device performance is a big concern in scaled CMOS technologies [1]. Double diffusion break (DDB) isolates neighboring devices with fin tuck under dummy poly shown in Fig. 1 (a), taking 1 poly pitch of width of shallow trench isolation (STI). Single diffusion break (SDB) is a promising option to reduce die area with STI width of 1 gate length illustrated in Fig. 1 (b), but a heavy facet of source/drain (S/D) epi at edge of STI causes epi volume reduction and drive current variation.

To investigate impact of DDB and SDB on S/D epi-induced stress and drive current, we apply TCAD process and Monte-Carlo (MC) device simulations. First, we demonstrate that the TCAD simulation results show a good agreement with Imec 14nm FinFET experimental data of the DDB. Using the validated TCAD setup, the stress and device performance of 7nm FinFET with the SDB are evaluated.

2. Double Diffusion Break in 14nm-node FinFET
Fig. 2 shows schematic views of Imec 14nm FinFET with 28nm gate length, 7nm fin width, 26nm fin height, 45nm fin pitch, 11nm gate spacer thickness, 110nm poly pitch and DDB structure. The length-of-oxide (LOD) represents a distance from edge of the center channel to the STI. We fabricated the devices having 3 different LOD, named LODn in which LOD equals to n*CPP-Lg/2, where CPP is poly pitch and Lg is physical gate length.

The TCAD process simulations run to estimate channel strain of the devices of LOD1, LOD2 and LOD3, considering only S/D epi-induced stress. The integrated channel strain in the center channel is plotted in Fig. 3. The strain increases from LOD1 to LOD2 by 25% approximately in both n- and p-FinFET. The channel closer to the STI suffers from stress relaxation more due to the proximity to free space at fin-cut edge at the STI oxide, that reduces stress due to small elastic stiffness. A small increase of the strain from LOD2 to LOD3 is observed since LOD2 is enough far from the STI to avoid the stress relaxation.

Taking the estimated strain value, the single-particle MC device simulation considering quasiballistic overshoot effects was performed with analytical dopant profile [2][3]. The simulated drain currents of the LOD1 at absolute drain voltage of 0.05V and 0.8V have been reasonably matched with the measured ones in the n- and p-FinFET as depicted in Fig. 4.

Fig. 3 Integrated channel strain in the center channel in 14nm FinFET.

Fig. 4 Measured and simulated drain currents of Imec 14nm FinFET

Fig. 5 shows the LDE on the drain current in the linear regime extracted at 0.4V threshold voltage offset. The measured LDE in n-FinFET is 2% increase of the drain current from LOD1 to LOD2, while 4% is found in the simulation. The p-FinFET pronounces the LDE due to silicon-germanium S/D epi stressor with 16% increase in the experiments and 11% in the simulation. In spite of incomplete device inspec-
tion and lack of measured stress values, the same trend between the measured and simulated results are obtained. That validates a reasonable accuracy of the TCAD simulation approach for device performance prediction.

3. Single Diffusion Break in 7nm-node FinFET

As technology scales towards 7nm node, the electrical impact of the SDB enabling die area reduction with narrowing STI width has to be investigated. Fig. 6 summarizes process flow assumption of the DDB and SDB. The DDB and non-self-aligned SDB can be made by the same flow, but the height of the oxide filled in the STI assumes to be different shown in Fig. 1.

The self-aligned SDB (SA-SDB) is formed after S/D epi growth and its width is defined by length of poly mask. On the other hand, the non-self-aligned SDB has a potential issue of misalignment between fin-cut and poly masks. Fig. 7 shows schematic views of 7nm FinFET with 18nm gate length, 5nm fin width, 35nm fin height, 24nm fin pitch, 5nm gate spacer thickness, 42nm poly pitch and the SDB structure. The fin tuck exists under the dummy poly and the S/D epi grows towards 3 facets of top and both sides in case of no misalignment. If fin-cut and poly masks are misaligned enough to make fin tuck in the S/D contact area, the S/D epi volume is significantly reduced due to extra facet towards edge of the fin. The epi shape is accurately predictable using the kinetic monte-carlo option in TCAD process simulation for epitaxial growth shown in Fig. 7(b) [4].

The SA-SDB removes a risk of the epi volume reduction thanks to alignment to dummy poly, but S/D epi-induced stress is lost during the STI formation similar to the DDB case. Fig 8 compares process simulation results of the LDE on the channel strain in the center channel of the DDB, SDB and SA-SDB as well as non-fin-cut as a reference. The DDB and SA-SDB decrease the strain by 85% at LOD1 compared to the non-fin-cut due to the stress relaxation during dummy poly removal. The SDB has benefit of retain the strain in the channel due to stiff environment around the S/D epi.

![Fig. 8 LDE on channel strain at center channel in 7nm FinFET](image)

Based on the simulated stress values, MC device simulations were run to assess drain current at supply voltage of 0.65V. The on-state drain currents with off-state current targeted to 0.1nA/µm in LOD1 are plotted in Fig. 9. Compared to non-fin-cut, the on-currents of the DDB and SA-SDB are degraded by 10% and 38% for n- and p-FinFET respectively. On the other hand, the SDB achieves high on-current due to no loss of the strain, however the on-current degradation of 9% in n-FinFET and 25% in p-FinFET in case of 5nm misalignment need to be taken into account.

4. Conclusion

We demonstrated that the TCAD MC device simulation results have successfully agreed with the experimental data of the 14nm FinFET LDE on on-state current with the DDB.

For a further scaling node, the validated TCAD deck has predicted the LDE of the SDB on channel strain and drain current. The non-self-aligned SDB can retain S/D epi-induced stress in the channel and achieve high drain current, but its variability due to mask misalignment needs to be considered. The SA-SDB has a benefit of variability and die area reduction in spite of lower drain current than the non-self-aligned SDB.

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References