Extended Abstracts of the 2017 International Conference on Solid State Devices and Materials, Sendai, 2017, pp221-222

Insights and Opportunities for Junctionless Gate-All-Around Lateral and Vertical Nanowire FETs

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Abstract

We report a comprehensive evaluation of junctionless (JL) gate-all-around (GAA) nanowire FETs (NWFETs) built in a lateral or vertical configuration *vs.* conventional inversion-mode (IM) devices. Focusing on accumulation-mode JL, a correlation between their lower oxide electric field (E_{ox}) values, reduced LF noise, and more uniform oxide trap density (N_{ot}) profiles is presented, while smaller Coulomb scattering coefficients (reduced with increasing NW doping, N_{NW}) agree with the predicted carriers distribution profiles. Other key points investigated are: 1) impact of the device dimensions and N_{NW} on the V_G dependence of gate capacitance (C_{GG}); 2) $R_{S/D}$-mobility trade-offs for boosting I_{ON} of JL; 3) similar time-zero and time-dependent variability for IM and JL devices for sufficiently low N_{NW} ($N_{NW} \leq 1\times10^{19}$ at/cm^3), with Monte Carlo simulations also showing that, in this case, quite comparable A_{VT} values can be achieved; and 4) improved A_{VT} and higher 6T-SRAM read stability (increased SNM) by relaxing the gate length (L_{gate}) of the cell pass-gate (PG) transistors, a feature which can be implemented without area penalty using vertical GAA-NWFETs.

1. Introduction

For advanced (sub-)5nm nodes, to continue the industry's growth rate and enable higher value systems, several options can be considered in regard to device architectures, material choices, integration approaches, and circuit designs. From a device perspective, GAA-NWFET, thanks to its superior electrostatics control, is widely considered one of the most promising candidates to further support the CMOS roadmap [1-3], whereas the JL concept [2-5] has been receiving increasingly more attention due to its attractive process simplicity, with demonstrated superior reliability and potential for low-power circuits and analog/RF applications [2,3]. In this work, we will further explore these devices with an in-depth investigation of their carrier density and electric field distributions, correlation with noise, N_{ot} profiles and NW doping *vs.* NW size, addressing also the areas of capacitance, parasitics and variability for optimized device/circuit performance. Moreover, as scaling of conventional 2D cell layouts is being challenged by the physical limits on gate and contact placement and interconnect routing congestion [6], looking into their potential for implementation in a vertical configuration appears particularly critical and timely to consider, namely by focusing on the extra opportunities it can allow for yielding higher performing scaled circuits, such as SRAMs, a topic which will also be here discussed.

2. Device fabrication

Schematics and examples of TEM images from the lateral and vertical GAA-NWFETs evaluated in this work are shown in Fig.1. While fabrication details can be found in [2,3,7], it is worthwhile to mention that JL channel doping was obtained by ion implantation (I/I) for lateral devices and by in-situ doped Si epi for VNWFETs. A similar HfO_2/TiN/W gate stack was used for all studied devices.

3. Results and discussion

Fig.2 shows the carriers density (holes in the case of PMOS) and electric field profiles for GAA-NWFETs with 10nm diameter (d_{NW}) wires, comparing IM *vs.* JL for various N_{NW}. The latter determines if the JL devices operate in accumulation or depletion mode (where the conduction peak occurs at the center of the wire). The carriers are closer to the interface for IM devices, with the charge distribution centroid moving further away from the interface with increasing N_{NW}. JL also exhibit smaller E_{ox} values, lower with increasing N_{NW}, with the expected reliability benefits previously confirmed in [2]. Fig.3 displays the simulated gate capacitance characteristics for various device architectures, IM *vs.* JL, with similarly highly-doped source/drain (S/D) areas. For curves calculated assuming I_{OFF}=100nA/μm (a-c): a weaker C_{GG}-V_G dependence is observed for JL with higher N_{NW}; a larger impact is seen for triple-gate finFETs (a) *vs.* GAA-NWFETs (c) (W_{Fin}= d_{NW}=10nm) due to the better electrostatic confinement provided by GAA. Also, since higher doping requires smaller NWs to be able to fully turn off the device, steeper C_{GG}-V_G curves are obtained for 10 *vs.* 30nm d_{NW} (c,b) for a given N_{NW}. As a lower C_{GG} helps reducing the intrinsic device delay, this could make it potentially interesting for some applications to explore the JL device geometry. For d_{NW}=10nm, similar CV curves are obtained (assuming fixed I_{OFF} or fixed effective workfunction (EWF)) for N_{NW} up to ~1×10^{19} at/cm^3 (c-d), agreeing with the experimental results shown in Fig.4.

Regarding JL drive currents, Fig.5 shows that, for uniformly doped wires, I_{ON} peaks at a certain NW doping concentration, which varies with d_{NW}, and is higher for smaller d_{NW}. As these devices are dominated by $R_{S/D}$, they face a mobility-$R_{S/D}$ trade-off, with I_{ON} increasing with N_{NW} until the resistance of the ungated areas no longer dominates. Introducing highly doped S/D areas helps reduce $R_{S/D}$ (and hence improve I_{ON}), especially for the smaller d_{NW} and lower N_{NW} devices but, as highlighted in Fig.6, the resistance of the region under the spacers also needs to be taken into account for I_{ON} optimization, with wider spacers requiring higher N_{NW} to compensate for it. These trends are experimentally confirmed in Figs.7 and 8, where a higher N_{NW} helps increase I_{ON} without impacting I_{OFF} (which is attractively lower than I_{OFF} of IM devices) for smaller wires, for both lateral and vertical NWFETs.

Overall, Fig.9 shows improved LF noise behavior for JL devices, with lower normalized input-referred noise spectral density values (measured for both N/PMOS) indicating less traps/defects present. Interestingly, the N_{ot} *vs.* trap depth comparison presented in Fig.10 for the various type of devices shows steeper profiles for IM, with their N_{ot} values increasing towards the metal gate and being higher than those for JL, for both P/NMOS. Previously, we reported on the impact of the EWF-metal on N_{ot}, with sloped profiles for TiN devices attributed to the occurrence of oxygen scavenging from the high-k layer by Ti, thus creating oxygen defects in the gate stack, while similar N_{ot} values were extracted at the Si/SiO_2 interface for different EWF-metals [8]. In Fig.10, since all devices have similar gate stacks, the lower JL E_{ox} values (varying with N_{NW}) are thought to cause the differences seen in active traps distributions. This is further corroborated by the smaller Coulomb scattering coefficients calculated in Fig.11 for JL *vs.* IM (lower for increasing N_{NW}), indicative of a longer distance of the carriers distribution centroid from the interface [9], in agreement with Fig.2. Variability-wise, Fig.12 shows that similar time-zero ($\sigma(V_{Tlin,0})$) and time-dependent variability ($\sigma(\Delta V_{Tlin})$, calculated from the data in Fig.12b as $\sigma^2(\Delta V_{Tlin})=2\eta<\Delta V_{Tlin}>$ at $<\Delta V_{Tlin}>$=50mV) can be obtained, using matched pair transistors [10,11], for IM and JL, provided N_{NW} is kept low enough, while Fig.13 demonstrates that smaller wires can allow wider ΔN_{NW} with less V_T impact. In addition, the Monte Carlo simulation results in Fig.14 confirm that low $\sigma(V_{Tlin})$ and mismatch (as quantified by the Pelgrom plot slope, A_{VT}) values, comparable to those of IM, can be obtained for JL with N_{NW} up to ~1×10^{19} at/cm^3, with advantages further predicted for longer L_{gate} devices. The latter is also a well-known way to improve the SRAM stability, namely by increasing the PG transistors L_{gate} to boost its read static noise margin (SNM) [12], as shown in Fig.15, where attractive performances of JL-based SRAMs are moreover visible. As VNWFETs can allow relaxed L_{gate} without area penalty, they appear thus particularly well suited for higher performing scaled SRAMs, with Fig.16 indicating that learnings on JL variability *vs.* N_{NW} and d_{NW} on lateral NWFETs also apply to vertical NWFETs.

4. Conclusions

A thorough evaluation of JL *vs.* IM GAA-NWFETs was pursued providing further insights into: carrier charge and electric field distributions, noise behavior and N_{ot} profiles, $C_{GG}(V_G)$, and their dependences on d_{NW} and N_{NW} (*vs.* finFET); JL I_{ON} improvement knobs; and variability, with relaxed L_{gate} for the SRAM PG devices attractive to implement with VNWFETs to improve SNM and A_{VT}.

References

[1] K. J. Kuhn, IEEE Trans. Elect. Dev., 59(7) (2012) 1813; [2] A. Veloso *et al.*, VLSI Tech. Dig. (2015) 138; [3] A. Veloso *et al.*, VLSI Tech. Dig. (2016) 138; [4] J.-P. Colinge *et al.*, Nature Nano. (2010) 225; [5] R. Rios *et al.*, IEEE Elect. Dev. Let., 32(9) (2011) 1170; [6] A. V.-Y. Thean *et al.*, VLSI Tech. Dig. (2015) 26; [7] A. Veloso *et al.*, ECS Trans., 72(4) (2016) 31; [8] W. Fang *et al.*, IEEE Elect. Dev. Let., 37(4) (2016) 363; [9] C. G. Theodorou *et al.*, ESSDERC Tech. Dig. (2012) 334; [10] B. Kaczer *et al.*, IEEE Elect. Dev. Let., 36(4) (2015) 300; [11] B. Kaczer *et al.*, IRPS Tech. Dig. (2017) 2D-6; [12] N. Collaert *et al.*, ICICDT Tech. Dig. (2008) 59.

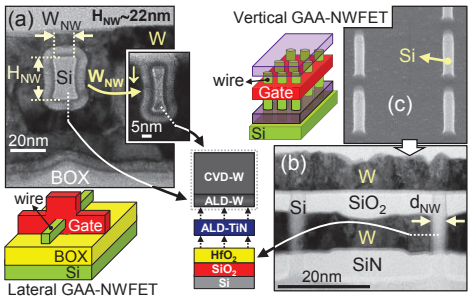


Fig.1 – Schematics and TEM images taken across wires after full device fabrication for (a) lateral and (b) vertical NWFET devices, with (c) showing a SEM image taken after the Si pillars patterning step in the VNWFETs flow.

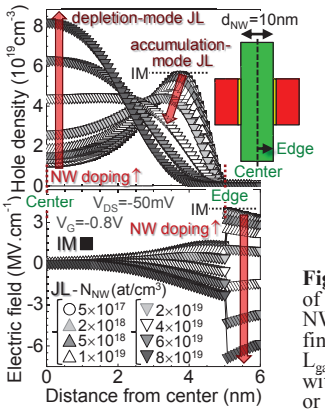


Fig.2 – TCAD evaluation of the carrier density and electric field profiles as a function of the NW doping for JL *vs.* IM GAA-NWFETs (PMOS case illustrated here).

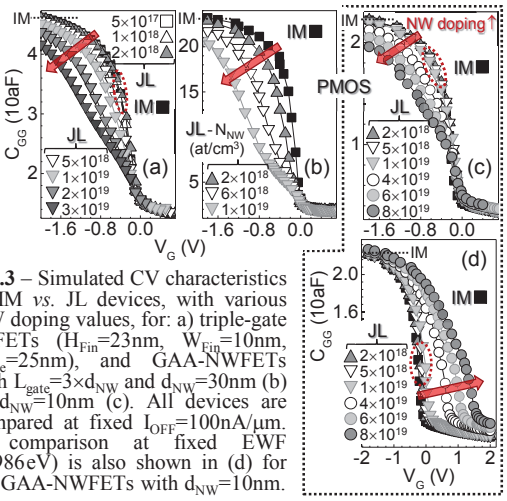


Fig.3 – Simulated CV characteristics of IM *vs.* JL devices, with various NW doping values, for: a) triple-gate finFETs (H_{Fin}=23nm, W_{Fin}=10nm, L_{gate}=25nm), and GAA-NWFETs with L_{gate}=3×d_{NW} and d_{NW}=30nm (b) or d_{NW}=10nm (c). All devices are compared at fixed I_{OFF}=100nA/μm. A comparison at fixed EWF (4.986eV) is also shown in (d) for the GAA-NWFETs with d_{NW}=10nm.

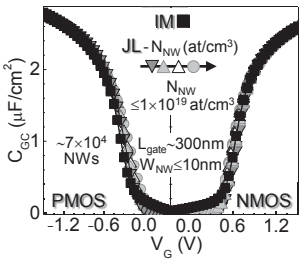


Fig.4 – Measured CV curves for IM *vs.* JL GAA-NWFET devices consisting of ~7×10^4 nanowires (H_{NW}~22nm, W_{NW}≤10nm) and L_{gate}~300nm. JL NW doping was targeted as ≤1×10^{19}at/cm^3, hence no significant differences in the shape of the curves are seen, in agreement with the TCAD results in Fig.3d.

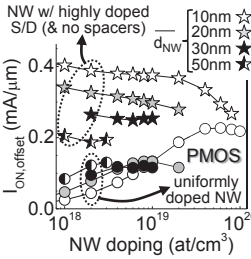


Fig.5 – TCAD evaluation of the impact of NW doping and NW size on I_{ON} at V_T overdrive (V_G-V_T= -0.7V, V_{DS}=-1.0V). The comparison is done at fixed I_{OFF}=100nA/μm, L_{gate}=3×d_{NW}.

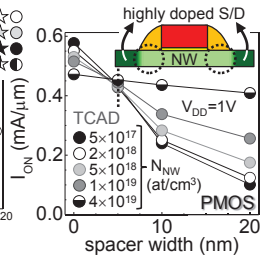


Fig.6 – For JL NWFETs w/ highly doped S/D areas, the NW doping in the regions under the spacers is also crucial for series resistance and I_{ON} tuning. For wider spacers, a $R_{S/D}$-mobility trade -off leads to N_{NW}↑ ⇒ I_{ON}↑.

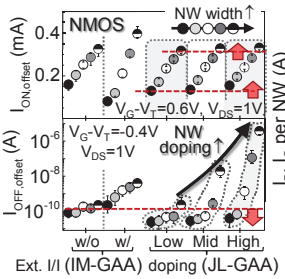


Fig.7 – I_{ON} and I_{OFF} at V_T overdrive for n-type IM (built w/ or w/o extension I/Is) *vs.* JL (N_{NW} ≤ 1×10^{19} at/cm^3) GAA-LNWFETs (L_{gate}~48nm, W_{NW} <25nm). For smaller NWs, JL exhibit lower I_{OFF}, with higher N_{NW} helping to boost I_{ON}, without impacting I_{OFF}, due to lower $R_{S/D}$ (as shown in Fig.6).

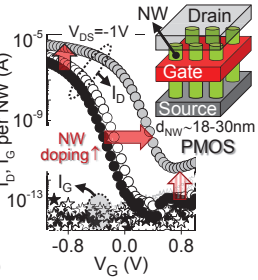


Fig.8 – IV characteristics of p-type JL GAA-VNWFETs, highlighting that increased NW doping leads to: I_{ON}↑, ΔV_T, and also I_{OFF}↑ for the larger NW devices (d_{NW} in the NWs arrays ~18-30nm).

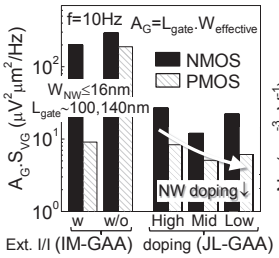


Fig.9 – Overall, lower LF noise values are measured for JL *vs.* IM GAA-LNWFETs for both NMOS and PMOS. A small noise dependence for JL on the NW doping (targeted here to be ≤1×10^{19}at/cm^3) is observed.

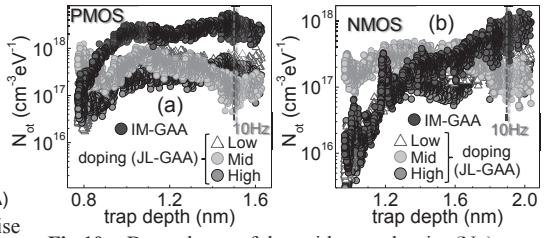


Fig.10 – Dependency of the oxide trap density (N_{ot}) on the trap depth for p- (a) and n-type (b) IM *vs.* JL GAA-LNWFETs built with similar gate stacks (W_{NW}<16nm, L_{gate}~140nm). In both cases, while IM show steeper profiles with their N_{ot} values increasing towards the metal gate, JL exhibit more uniform profiles and lower N_{ot} values, linked to the N_{NW} used (≤1×10^{19}at/cm^3).

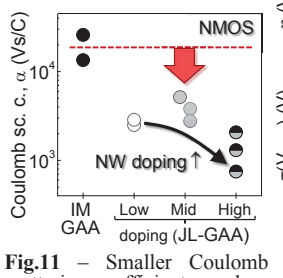


Fig.11 – Smaller Coulomb scattering coefficient α values are calculated for JL *vs.* IM devices, being lower for N_{NW}↑ and indicative of the distance of the carriers distribution centroid from the interface, in good agreement with Fig.2.

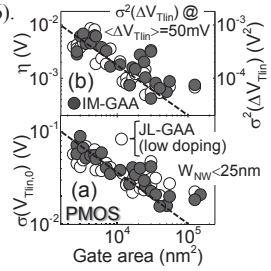


Fig.12 – Similar time-zero ($\sigma(V_{Tlin,0})$ in (a)) and time-dependent ($\sigma(\Delta V_{Tlin})$ in (b)), as expressed by the mean impact of a single trap η) variability are extracted for IM and JL, provided the JL N_{NW} is low enough.

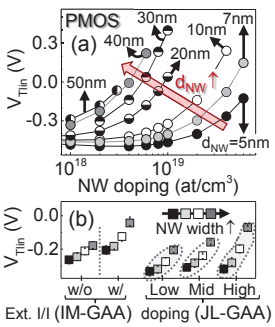


Fig.13 – TCAD results in (a) show that V_T modulation by NW doping is more pronounced for larger NWs, with d_{NW}↓ allowing a wider process window for V_T control. This is confirmed experimentally in (b), where W_{NW}<25nm.

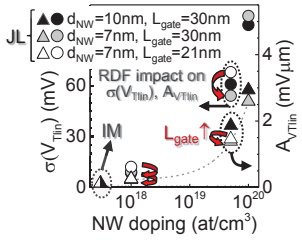
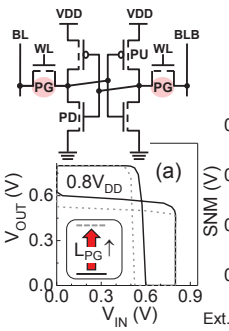


Fig.14 – Monte Carlo simulations confirm expected trend of higher V_T variability with increased N_{NW} for JL GAA-NWFETs due to RDF. Acceptably low A_{VT} values can still be obtained for N_{NW} up to ~1×10^{19}at/cm^3, while there is also a clear advantage for devices with a longer L_{gate}.



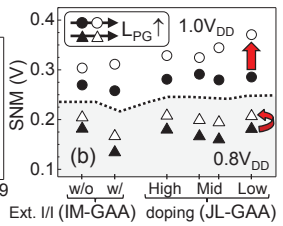


Fig.15 – 6T-SRAM cells with a higher β ratio (hence improved read stability) can be obtained by increasing the L_{gate} of the PG transistors. This is illustrated by the increased eye of the butterfly curves in (a) and by the median SNM values in (b), also showing attractive performances for the simpler JL-based SRAMs.

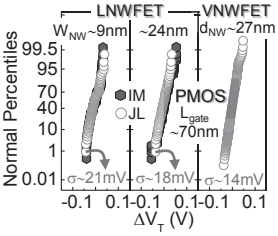


Fig.16 – ΔV_T of JL NWFETs with similar N_{NW}, in lateral or vertical configurations. The latter are particularly attractive for SRAM stability and scaling since they allow relaxed L_{gate} without area penalty.