Insights and Opportunities for Junctionless Gate-All-Around Lateral and Vertical Nanowire FETs
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Abstract
We report a comprehensive evaluation of junctionless (JL) gate-all-around (GAA) nanowire FETs (NWFETs) built in a lateral or vertical configuration vs. conventional inersion-mode (IM) devices. Focusing on accumulation-mode JL, a correlation between their lower oxide electric field (Eox) values, reduced LF noise, and more uniform oxide trap density (Nt) profiles is presented, while smaller Coulomb scattering coefficients (reduced with increasing NW doping, NNW) agree with the predicted carrier distributions. Other key points investigated are: 1) impact of the device dimensions and NNW on the Vth dependence of gate capacitance (CGG); 2) Rs-RdL-technology trade-offs for boosting Ion of JL; 3) similar time-zero and time-dependent variability for IM and JL devices for sufficiently low NNW (NNW < 1x10^18 cm^-3) with Monte Carlo simulations also showing that, in this case, quite comparable ACT values can be achieved, and 4) improved AVAT and higher 6σ SRAM read stability (increased SNM) by relaxing the gate length (Lg) of the cell pass-gate (PG) transistors, a feature which can be implemented without area penalty using vertical GAA-NWFETs.

1. Introduction
For advanced (sub-)5nm nodes, to enable higher value systems, several options can be considered in regard to device architectures, material choices, integration approaches, and circuit designs. From a device prospective, GAA-NWFETs, thanks to its superior electrostatics control, is widely considered one of the most promising candidates to further support the CMOS roadmap [1-3], whereas the JL concept [2-5] has been receiving increasingly more attention due to its attractive process simplicity, with demonstrated superior reliability and potential for low-power circuits and analog/RF applications [2,3]. In this work, we will further explore these devices with an in-depth investigation of their carrier density and electric field distributions, correlation with noise, Nt profiles and NW doping vs. NW size, addressing also the areas of capacitance, parasitics and variability for optimized device/circuit performance. Moreover, as scaling of conventional 2D cell layouts is being challenged by the physical limits on gate and contact placement and interconnect routing congestion [6], looking into their potential for implementation in a vertical configuration appears particularly critical and timely to consider, namely by focusing on the extra opportunities it can allow for yielding higher performing scaled circuits, such as SRAMs, a topic which will also be here discussed.

2. Device fabrication
Schematics and examples of TEM images from the lateral and vertical GAA-NWFETs evaluated in this work are shown in Fig.1. While fabrication details can be found in [2,3], it is worth mentioning that JL channel doping was obtained by ion implantation (I/I) for lateral devices and by in-situ doped Si epi for VNWFETs. A similar HfO2/TiN/W gate stack was used for all studied devices.

3. Results and discussion
Fig.2 shows the carriers density (holes in the case of PMOS) and electric field profiles for GAA-NWFETs with 10nm diameter (dNW) wires, comparing IM vs. JL for various NNW. The latter determines if the JL devices operate in accumulation or depletion mode (where the conduction peak occurs at the center of the wire). The carriers are closer to the interface for IM devices, with the charge distribution centroid moving further away from the interface with increasing NNW. JL also exhibit smaller Eox values, lower with increasing NNW, with the expected reliability benefits previously confirmed in [2]. Fig.3 displays the simulated gate capacitance characteristics for various device architectures, IM vs. JL, with similarly highly-doped source/drain (S/D) areas. For curves calculated assuming Ion=100nA/μm (a-c): a weaker CGG-Vth dependence is observed for JL with higher NNW; a larger impact is seen for triple-gate finFETs (a) vs. GAA-NWFETs (c) (Vth= dNW=10nm) due to the better electrostatic confinement provided by GAA. Also, since higher doping requires smaller NWs to be able to fully turn off the device, steeper CGG-Vth curves are obtained for 10 vs. 30nm dNW (b,c) for a given NNW. As a lower CGG helps reducing the intrinsic device delay, this could make it potentially interesting for some applications to explore the JL device geometry. For dNW=10nm, similar CV curves are obtained (assuming fixed Ioff or fixed effective workfunction (EWF)) for NWW up to ~1x10^19 cm^-3 (c-d), agreeing with the experimental results shown in Fig.4. Regarding JL drive currents, Fig.5 shows that, for uniformly doped wires, Ion peaks at a certain NW doping concentration, which varies with dNW, and is higher for smaller dNW. As these devices are dominated by RdL, they face a mobility-RdL trade-off, with Ion increasing with NWW until the resistance of the ungated areas no longer dominates. Introducing highly doped S/D areas helps reduce RsD (and hence improve Ion), especially for the smaller dNW and lower NNW devices but, as highlighted in Fig.6, the resistance of the region under the spacers also needs to be taken into account for Ion optimization, which is a feature higher NNW to compensate for. These trends are experimentally confirmed in Figs.7 and 8, where a higher NWW helps increase Ion without impacting IOFF (which is attractively lower than IOFF of IM devices) for smaller wires, for both lateral and vertical NWFETs.

Overall, Fig.9 noise behavior and with lower normalized input-referred noise spectral density values (measured for both N/PMOS) indicating less traps/defects present. Interestingly, the NWW vs. trap depth comparison presented in Fig.10 for the various type of devices shows steeper profiles for IM, with their NWW values increasing more modestly towards the metal gate than those for JL, for both N/PMOS. Previously, we reported on the impact of the EWF-metal on Nt, with sloped profiles for TN devices attributed to the occurrence of oxygen scavenging from the high-k layer by Ti, thus creating oxygen defects in the gate stack, whereas similar Nt values were obtained for the metal gate for different EWF-metals [8]. In Fig.10, since all devices have similar gate stacks, the lower JL Eox values (varying with NNW) are thought to cause the differences seen in active traps distributions. This is further corroborated by the smaller CGG-Vth scattering coefficients calculated in Fig.11 for JL vs. IM (lower for increasing NWW), indicative of a longer distance of the carriers distribution centroid from the interface [9], in agreement with Fig.2. Variability-wise, Fig.12 shows that similar time-zero (σ<sup>Vth</sup>lin) and time-dependent variability (σ<sup>Vth</sup>lin) trends are observed for both P/NMOS. Interestingly, the Not values increasing towards the metal gate and being higher for the various type of devices shows steeper profiles for IM, with their Not values increasing more modestly towards the metal gate than those for JL, for both N/PMOS. In Fig.12b, as σ<sup>Vth</sup>lin=2σ<sup>N</sup>eng at <CVthlin>~50mV) can be obtained, using matched pair transistors [10,11], for IM and JL, provided NWW is kept low enough, while Fig.13 demonstrates that smaller wires can widen NWW with less Vt impact. In addition, the Monte Carlo simulation results in Fig.14 confirm that lower Nt, as well as mismatch (as quantified by the Pelgrom plot slope, AVAT) values, compared to those of IM, can be obtained for JL with NWW up to ~1x10^18 cm^-3, with advantages further predicted for longer Lg devices. The latter is also a well-known way to improve the SRAM stability, namely by increasing the PG transistors Lg without affecting its read static noise margin (SNM) [12], as shown in Fig.15, where attractive performances of JL-based SRAMs are moreover visible. As NWFETs can allow relaxed Lg without area penalty, they appear thus particularly well suited for higher performing scaled SRAMs, with Fig.16 indicating that learning on JL variability vs. NNW and dNW on lateral NWFETs also apply to vertical NWFETs.

4. Conclusions
A thorough evaluation of JL vs. IM GAA-NWFETs was pursued providing further insights into: carrier charge and electric field distributions, noise profiles and variability, and Nt. Improvements in terms of lower oxide electric field (Eox) values, reduced LF noise, and more uniform oxide trap density (Nt) profiles are presented, while smaller Coulomb scattering coefficients (reduced with increasing NW doping, NNW) agree with the predicted carrier distributions. Other key points investigated are: 1) impact of the device dimensions and NNW on the Vth dependence of gate capacitance (CGG); 2) Rs-RdL-technology trade-offs for boosting Ion of JL; 3) similar time-zero and time-dependent variability for IM and JL devices for sufficiently low NNW (NNW = 1x10^18 cm^-3) with Monte Carlo simulations also showing that, in this case, quite comparable ACT values can be achieved, and 4) improved AVAT and higher 6σ SRAM read stability (increased SNM) by relaxing the gate length (Lg) of the cell pass-gate (PG) transistors, a feature which can be implemented without area penalty using vertical GAA-NWFETs.

References
Fig.1 – Schematics and TEM images taken across wires after full device fabrication for (a) lateral and (b) vertical NWFET devices, with (c) showing a SEM image taken after the Si pillars patterning step in the VNWFTs flow.

Fig.2 – TCAD evaluation of the carrier density and electric field profiles as a function of the NW doping for JL vs. IM GAA-NWFETs (PMOS case illustrated here).

Fig.3 – Simulated CV characteristics of IM vs. JL devices, with various NW doping values, for: (a) triple-gate finFETs (HNW =25nm, WN=10nm) and (b) single-gate IM-GAA-NWFETs (PMOS case illustrated here).

Fig.4 – Measured CV curves for IM vs. JL GAA-NWFET devices consisting of ~7x10^4 nanowires (HNW =25nm, WN=10nm) and Lgate=300nm. JL NW doping was targeted at ~1x10^19/cm^2, hence no significant differences in the shape of the curves are seen, in agreement with the TCAD results in Fig.3d.

Fig.5 – TCAD evaluation of the impact of NW doping and NW size on ION vs. VGS overdrive for JL (a) and IM (b) devices, being lower for IM due to thinner oxide in the spacer region.

Fig.6 – NW doping profiles for IM and JL, providing insights on the width of the junctions.

Fig.7 – ION and VGS values from IM and JL devices with NWs (dNW) =30nm and (dNW) =10nm. For smaller NWs, JL exhibit lower ION, with higher NWW helping to boost ION without impacting IOFF, due to lower RSD (as shown in Fig.6).

Fig.8 – IV characteristics of n-type JL GAA-NWFETs highlighting that increased NW doping leads to L vs. I, I vs. ΔV, and also IOFF for the larger NW devices (dNW) in the NWs arrays =18-30nm.

Fig.9 – Overall, lower LF noise values are measured for JL vs. IM GAA-LNWFTEs for both NMOS and PMOS. A small noise dependence for JL on the NW doping (targeted here to be 3x10^19/cm^2) is observed.

Fig.10 – Dependency of the oxide trap density (Nt) on the trap depth for p- and n-type (b) IM vs. JL GAA-LNWFTEs built with similar gate stacks (WN=16nm, Lgate=140nm). In both cases, while IM show steeper profiles with their Nt values increasing towards the metal gate, JL exhibit more uniform profiles and lower Nt values, linked to the Nww used (1x10^19/cm^2).

Fig.11 – Smaller Coulomb scattering coefficient μ values are calculated for JL vs. IM devices, being lower for NW in and indicative of the distance of the carriers distribution centroid from the interface, in good agreement with Fig.2.

Fig.12 – Similar time-zero (τ0) and time-dependent (τn) in (a) and (b), as expressed by the mean impact of a single trap μ, is 100% for IM and JL, provided the JL Nww is low enough.

Fig.13 – TCAD results in (a) show that Vt modulation by NW doping is more pronounced for larger NWs, with dww allowing a wider process window for Vt control. This is confirmed experimentally in (b), where Vt vs. (a).

Fig.14 – Monte Carlo simulations confirm expected trend of higher Vt variability with increased NW doping for JL GAA-LNWFTEs due to RDF. Acceptably low Vt values can still be obtained for Nww up to ~1x10^19/cm^2, while there is also a clear advantage for devices with a longer Lgate.

Fig.15 – 6T-SRAM cells with a higher β ratio (hence improved read stability) can be obtained by increasing the Lgap of the PG transistors. This is illustrated by the butterfly curves in (a) and the median SNM values in (b), also showing attractive performances for the simpler JL-based SRAMs.

Fig.16 – ΔVt of JL NWFTEs with similar Nww to lateral or vertical configurations. The latter are particularly attractive for SRAM stability and scaling since they allow relaxed Lgap without area penalty.