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High Performance Top-Gate Zinc Oxide Thin Film Transistor (ZnO TFT) by Combination of Post Oxidation and Annealing

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Abstract
Control of TiN/Al_2O_3/ZnO gate stacks by combination of post plasma oxidation and annealing have been demonstrated for top-gate TFTs with a thin (~10 nm) ZnO channel layer. Development of the interfacial control technique with understanding impacts of these treatments realized superior TFT performance with large ON/OFF, steep sub-threshold characteristics, and high field-effect mobility comprehensively.

1. Introduction

A Zinc oxide (ZnO) based thin film transistor (TFT) has high potential not only for display application but also LSI application because of its high electron mobility and low off-state current [1-2]. For a down-sized high performance TFT with a nano-meter-thick ZnO layer, importance of precise control of the interface between gate oxides and ZnO layers is significantly growing. Gate oxide formation by atomic layer deposition (ALD), which is commonly used for the advanced LSI technology, causes reductive reaction of oxides on substrate surfaces, which can be more critical for oxide semiconductors than conventional Si, Ge or III-V compounds [3]. We have previously demonstrated that plasma oxidation after high-k deposition can terminate defects at the high-k/semiconductor interfaces, reducing the interfacial state density [4-5]. Therefore, oxidation and/or thermal treatments after gate oxide deposition including such techniques are expected to realize superior gate-oxide/ZnO interfaces with low defect density.

In this study, we have investigated the impact of several post oxidation and annealing treatments on TFT operation in detail and have realized comprehensively superior TFT performances by reducing the defect density with post oxidation and annealing.

2. Fabrication of top-gate ZnO TFT

The fabrication process of top-gate ZnO TFTs is summarized in Fig. 1. A ZnO thin layer (11-13 nm) was deposited on a SiO_2/Si substrate by pulsed laser deposition (PLD) at 200°C, followed by annealing at 400°C. It was confirmed that the relatively smooth surface was obtained even after annealing (Fig. 2). An Al_2O_3 gate oxide was deposited by atomic layer deposition (ALD) at 200°C and its total thickness was 10 nm. During or after the Al_2O_3 deposition, *ex-situ* post plasma oxidation (PPO) and/or post O_2 annealing (POA) were performed at room temperature and 350°C, respectively. After TiN gate and Al source/drain formation, post metallization annealing (PMA) was carried out in N_2 ambient.

3. Results and discussion

Figure 3 shows I_d-V_g characteristics of a ZnO TFT with various oxygen treatments (a) without and (b) with PMA at 300°C, measured at room temperature. While cutting off of I_d is generally hard, PPO can effectively realize this. However, PPO largely decreases I_d. In contrast, POA increases I_d regardless of PPO and, thus, POA is essential for high I_{ON}. By the combination of PPO, POA, and PMA, large and steep ON/OFF transient (>10^7) were achieved.

The role of each treatment on the TFT performance is examined independently. Figure 4 shows *C*-*V* characteristics of a TiN/Al_2O_3/ZnO lateral-shaped MOS capacitor (as described in the inserted figure) after parasitic resistance correction, with (a) POA, (b) POA+PMA, (c) PPO+POA, and (d) PPO+POA+PMA. The capacitance of the samples without PPO ((a) and (b)) is hardly modulated by V_g. In contrast, the surface potential of the ZnO layer with PPO+POA+PMA is steeply modulated, supporting the superior ON/OFF of the TFT. Therefore, it is suggested that PPO can effectively release Fermi level pinning near the conduction band edge. Note here that charge compensation in the oxygen-rich or defect-induced ZnO layer may cause the reduction of the effective carrier concentration. On the other hand, resistivity reduction is observed after POA (Fig. 5), supporting larger I_{ON} of the TFT. It is speculated that improvement of ZnO crystallinity and/or defect termination at the grain boundary mitigates the charge compensation and/or improves carrier mobility [6], although careful investigation will be needed for detailed understanding. In contrast, PMA decreases the effective carrier concentration, which is attributable to charge compensation caused by oxygen abstraction. In particular, the influence of PMA has strong temperature dependence and the optimized temperature (~300°C) has realized the effective carrier concentration suitable for cutting off I_d of TFT with keeping high crystalline quality (Fig. 6).

The performance of the TFT with PPO+POA+PMA (at 300°C) was evaluated in detail. The I_d-V_g characteristics of the TFT with longer L_g are cut off by weaker V_g. Also, clear I_d saturation can be found in the wide V_g range (Fig. 8). The peak value of the field-effect mobility (peak μ_{FE}) increases with larger L_g and smaller W, *i.e.*, with larger channel resistance (Fig. 9). As a result, μ_{FE} of at least ~50 $cm^2/V{\cdot}s$ can be achieved by the appropriate combination of post oxidation and annealing. It should be highlighted that this μ_{FE} value is comparable to the highest one of bulk poly-ZnO [7]. S.S. as a function of I_d shows similar trend for TFTs with various L_d and the minimum value of as small as 130 mV/dec. was achieved (Fig. 10). Finally, the performance of TFTs with a poly-ZnO thin layer is benchmarked in Table I [8-11]. It can be concluded that present control of defects both at Al_2O_3/ZnO interface and in ZnO layer is essential for steep-slope TFT performance with high mobility and that the appropriate combination of post oxidation and annealing processes are quite important for TFT characteristics.

4. Conclusion

Impact of post oxidation and annealing of TiN/Al_2O_3/ZnO gate stacks on TFT performance has been systematically investigated. It is found that control of the ALD-Al_2O_3/ZnO interface is essentially important for superior ON/OFF operation of TFTs. The appropriate combination of PPO, POA, and PMA can realize remarkably high μ_{FE} (50 $cm^2/V{\cdot}s$) in top-gate TFTs with very thin (~10 nm) ZnO channel layers.

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References: [1] A. Tsukazaki *et al.*, J. Phys. D: Appl. Phys. **47**, 034003 (2014). [2] D. Matsubayashi *et al.*, Tech. Dig. IEDM 2015, p. 141. [3] C. L. Hinkle *et al.*, Microelec. Eng. **86**, 1544 (2009). [4] R. Zhang *et al.*, Appl. Phys. Lett. **98**, 112902 (2011). [5] K. Kato *et al.*, Jpn. J. Appl. Phys. **52**, 04CA08 (2013). [6] A. F. Kohan *et al.*, Phys. Rev. B **61**, 15019 (2000). [7] K. Ellmer *et al.*, Thin Solid Films **516**, 4620 (2008). [8] J. Nishii *et al.*, Jpn. J. Appl. Phys. **42**, L347 (2003). [9] T. Hirao *et al.*, J. Sci. Inf. Disp. **15**, 17 (2007). [10] H. Bong *et al.*, Appl. Phys. Lett. **96**, 192115 (2010). [11] Y. V. Li *et al.*, IEEE Elec. Dev. Lett. **34**, 891 (2013).

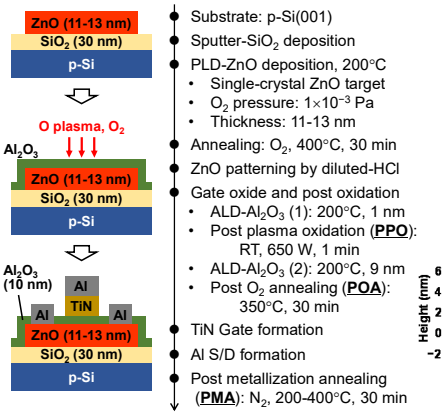

Fig. 1 Fabrication process and structure of top-gate ZnO TFT.

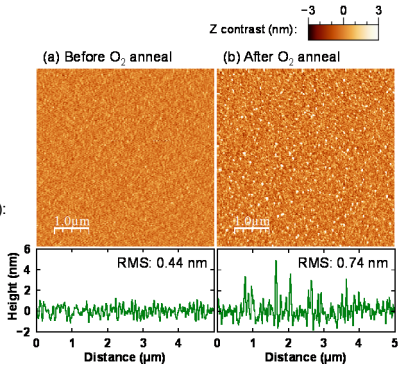

Fig. 2 AFM images of ZnO/Si (a) before and (b) after O_2 annealing at 400°C.

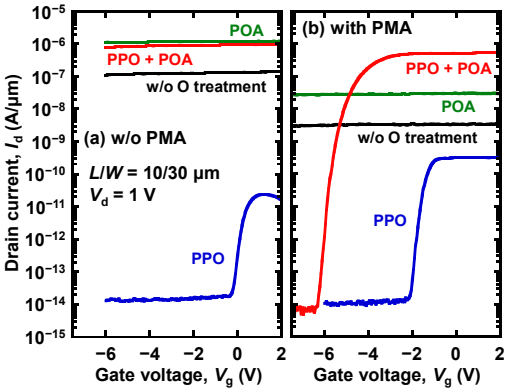

Fig. 3 I_d-V_g characteristics of ZnO TFT with various post treatments, (a) without and (b) with PMA.

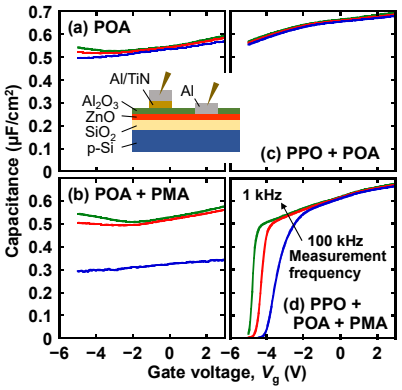

Fig. 4 *C-V* characteristics of TiN/Al_2O_3/ZnO MOS capacitors.

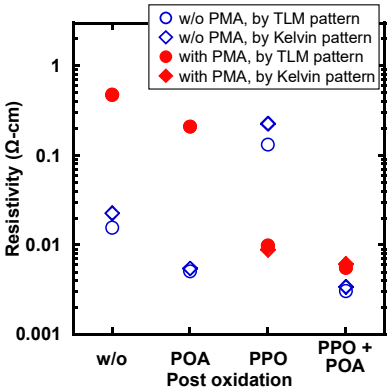

Fig. 5 Resistivity of ZnO thin layer with various post treatments.

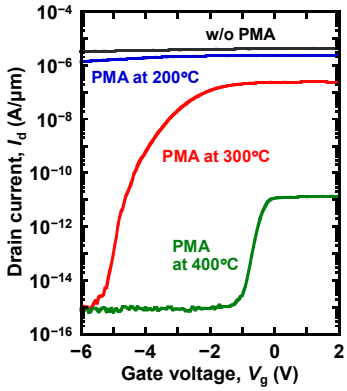

Fig. 6 I_d-V_g characteristics of ZnO TFT with various PMA temperatures.

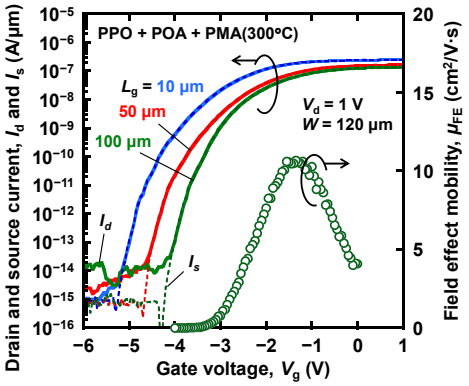

Fig. 7 I_d-(I_s-) V_g characteristics and μ_{FE} of ZnO TFT with various L_g.

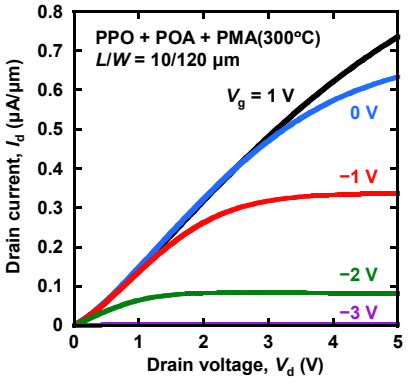

Fig. 8 I_d-V_d characteristics ZnO TFT after PMA with various V_g.

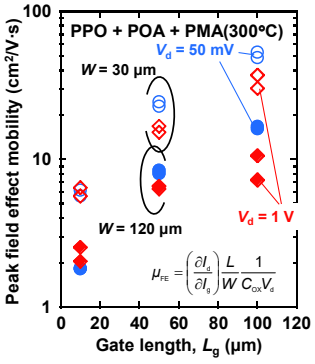

Fig. 9 Peak μ_{FE} of ZnO TFT as a function of L_g.

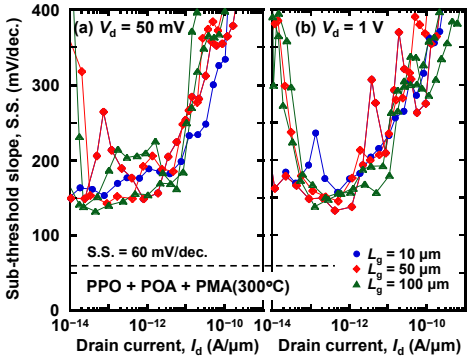

Fig. 10 *S.S. vs.* I_d of ZnO TFT with various L_g measured at V_d of (a) 50 mV and (b) 1 V.

Table I Benchmark of structure and performance TFT with poly-ZnO thin channel.

Group	Tohoku Univ	Kochi Univ. of Tech.	POSTECH	Penn state Univ.	**This work**
d_{ZnO} (nm)	100	65	10	10	**13**
Deposition	PLD	Sputter	sol-gel	PEALD	**PLD**
Top/Bottom	Bottom	Top	Top	Top/Bottom (Double)	**Top**
High-k	SiN/CaHfO	SiN	Ion gel	Al_2O_3	**Al_2O_3**
d_{High-k} (nm)	340/30	350	—	32/32	**10**
V_{th} (V)	~10	2	0.85	2	**−3**
I_{ON}/I_{OFF}	>10^7	>10^7	>10^5	>10^7	**>10^7**
μ_{FE} (cm²/V·s)	5	50	15	33	**50**
S.S. (mV/dec.)	1300	210	—	140	**130**
Reference	[8]	[9]	[10]	[11]	**—**
Year	2003	2007	2010	2013	**—**