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Performance evaluation of III-V nanowire broken-gap TFETs including electron-phonon scattering using an atomistic mode space NEGF technique enabling million atoms NW simulations.

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Abstract

Using an innovative atomistic mode space (MS) NEGF technique, we have demonstrated the capability to simulate in a quantum mechanical tight-binding (TB) atomistic fashion III-V NW devices featuring up to millions of atoms with large speed up (up to 10,000×) and good accuracy. Here, we review and extend our previous results including a validation of our MS method to experimental results and an in-depth atomistic study of the scaling potential of III-V GAA nanowire heterojunction n and pTFETs, including the impact of electron-phonon scattering, quantifying the benefits of this technology for low-power, low-voltage CMOS application.

1. Introduction

III-V gate-all-around (GAA) nanowire (NW) heterojunction TFETs (HTFET) can potentially replace conventional Si MOSFETs as a low power (LP) sub-10 nm technology option [1,2]. Despite the progress in the field [1], no experimental verification of sub-10 nm diameter (d) GAA NW III-V HTFET performance has been reported. Accurate and predictive modeling of III-V NW TFETs with technology relevant dimensions requires full-band quantum transport studies such as atomistic tight binding (TB) simulations within the NEGF framework [2,3,4]. Due to their computational cost, these simulations are difficult to afford using a traditional real space (RS) technique (Fig. 1) [2].

2. Tight-Binding Mode Space Model

Using an atomistic mode space NEGF technique showing large speed up and good accuracy against RS simulation results, we have reported the capability to simulate in a quantum mechanical tight-binding (TB) atomistic fashion III-V NW devices featuring several hundred thousands of atoms and diameter up to 7 nm [2,5,6]. The MS algorithm was implemented in the NEMO5 simulation tool [4]. We demonstrate here the capability to simulate millions of atoms NW with diameter up to 18 nm and speed up > 10,000× (Fig. 1).

The technique is very efficient and enables large reduction ratios of the Hamiltonian size, hence large speedup and memory reduction while keeping good accuracy (error < 1% when comparing to RS simulations) providing the MS bases are cleaned from unphysical modes [3,5,6,7].

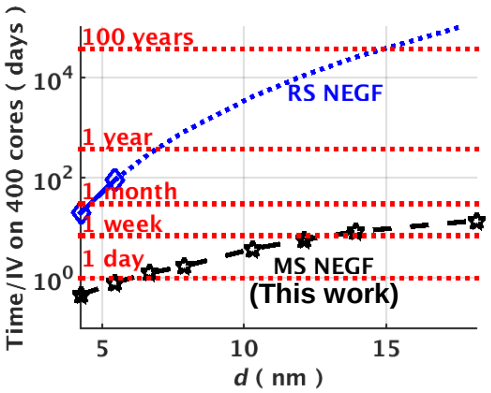

Fig. 1 Simulation time per IV to simulate an InAs/GaSb NW TFET vs. diameter d using a real space vs. mode space NEGF and a sp^3s^*SO (SO = spin-orbit coupling) TB basis Hamiltonian on a 400 cores cluster. RS NEGF time values are measured for d = 4 and 5.5 nm and extrapolated using a d^6 law for larger d [7].

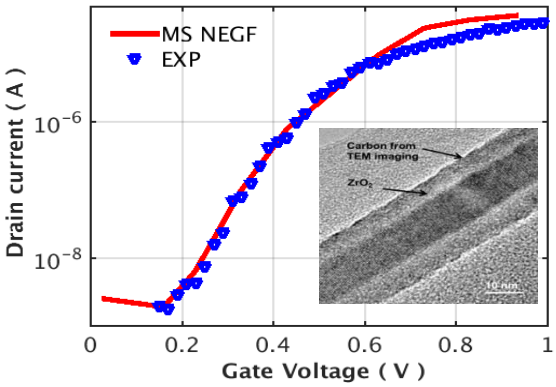

Fig. 2 $I_D(V_G)$ characteristics of a [111] d =12 nm InAs nMOS transistor measured and simulated using a ballistic TBMS – NEGF model from an optimized $sp^3s^*\_SO$ InAs MS basis. V_D = 0.5V. L = 300 nm. Inset: High-resolution TEM image along a NW.

Here, we also compare [111] d = 12 nm InAs NW nMOSFET experimental (see [8] for details) vs. simulated MS ballistic data on Fig. 5. Good agreement of the BTBT current and the subthreshold characteristics is observed. In the on-state, we extract a typical ballistic ratio of r = 75% for the 300 nm long InAs device.

3. Performances of Broken Gap TFETs

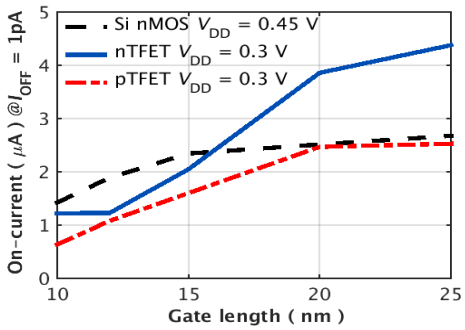

Fig. 3 Impact of gate length on I_{ON} (current /wire) of optimized InAs/GaSb GAA NW n- and pTFETs and Si GAA NW nMOSFETs. Gate oxide: 1.8 nm Al_2O_3 oxide. I_{OFF} = 1 pA/ wire, V_{DD} = 0.3 V for the TFETs and 0.45 V for the MOSFET.

We also reported the first in-depth atomistic optimization study of III-V GAA NW HTFET from a scaling perspective with d in the 4 - 7 nm range, L in the 10 to 25 nm range and crystal orientation dependence. Impact of material choice and architecture was also considered by adding an InGaAs heterojunction [2]. The study was enabled by our TB MS technique. Fig. 3 shows the evolution of on-current (I_{ON}) vs. gate length (L) for optimized ideal InAs/GaSb heterojunction n- and pTFETs and Si n MOSFETs when scaling L from 25 to 10 nm [2]. For the TFETs, we used ballistic simulations, which is a good approximation as we will demonstrate below (Fig. 4). Scattering was considered for the MOSFETs [9]. For each L a full optimization was performed.

As can be seen from Fig. 3, TFET performance degrades quite significantly and faster than that of Si MOSFETs when scaling L below 20 nm. The main reasons for the stronger degradation in the TFET cases are identified as follows. 1) More pronounced short channel effects, in particular a "source-to-drain" tunneling (SDT) effect as L is reduced below 20 nm. 2) A NW diameter of about 5.5 nm, which is optimal for controlling the TFET short channel effects at L = 20 nm, also yields optimally balanced InAs/GaSb material properties for the TFET application [2]. As a consequence, both n- and pTFET performances are best above 20 nm gate length for a diameter of 5.5 nm which features the best trade-off between electrostatic control and confinement effects. Such a configuration could benefit from up to 50% gain in the [111] crystal orientation at V_{DD} = 0.3 V and I_{OFF} = 50 pA/μm. In a LP ITRS 2.0 horizontal GAA beyond 5 nm node design rule however, where the gate length is restricted to 12 nm, a [100] orientation is best, but features 2.3 to 3× I_{ON} degradation and 1.9 to 2.4× energy-delay product (ETP) degradation compared to the 20 nm GAA design. The 20 nm GAA TFET design features I_{ON} and ETP performance gain over a Si NW MOSFET of 58× and 56× respectively [2].

In order to verify that the TFET steep swing is not degraded by electron-phonon scattering which is a fundamental source of non-idealities, we investigate the impact of electron-phonon scattering on optimized L = 20 nm nTFETs. We modeled electron – phonon scattering within the self-consistent Born approximation using an efficient form factor mode space NEGF algorithm [9]. With scattering electrons can relax their energy which potentially increases the probability of final tunneling states and tunneling current but may also decrease SS. $I_D(V_G)$ characteristics of the optimized L = 20 nm PNIN design including acoustic, optical and polar optical phonon within a local approximation are compared to the ballistic ones for various diameters in Fig. 4. As can be seen, SS and performance are not degraded compared to ballistic case in the relevant current range for low power CMOS application.

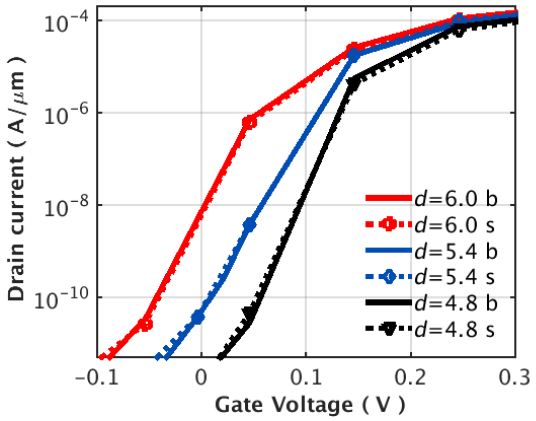

Fig. 4 $I_D(V_G)$ characteristics of optimized L = 20 nm InAs/GaSb GAA NW nTFETs with d = 4.8, 5.4 and 6 nm, simulated using a TBMS – NEGF model with (s, dashed lines with symbol) and without (b, plain lines) electron-phonon scattering from optimized $sp^3s^*\_SO$ InAs and GaSb MS bases. V_D = 0.3V. The work function of the TFETs were adjusted so that I_{OFF} of the d =5.4 nm device is 50 pA/um at V_G = 0V.

4. Conclusions

We have demonstrated here the capability to simulate in a quantum mechanical tight-binding (TB) atomistic fashion III-V NW devices featuring up to millions of atoms using a mode space (MS) NEGF technique. We also reviewed and extended our previous results including a validation of our MS method to experimental results and an in-depth atomistic study of the scaling potential of III-V GAA nanowire heterojunction n and pTFETs, including the impact of electron-phonon scattering, quantifying the benefits of this technology for low-power, low-voltage CMOS application.

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