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Investigation of TFETs with Vertical Tunneling Path for Low Average Subthreshold Swing

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Abstract

In this paper we analyze the capabilities in terms of average subthreshold swing and on-current of $Si_{0.50}Ge_{0.50}$/Si heterostructure n-TFETs with vertical tunneling path, utilizing an air bridge design to minimize source-drain leakage. We show that the on-current is line tunneling dominated and proportional to the source-gate overlap area. In order to obtain a low average subthreshold swing the onsets of diagonal point tunneling and line tunneling have to be merged closely, which is best achieved with a moderate counter doping in the channel. As a result average slopes of 87 mV/dec over 4 decades of I_d and I_{on}/I_{off} ratios of larger than 10^6 are obtained.

1. Introduction

The approach of reducing power consumption in integrated circuits by lowering the supply voltage, V_{dd}, demands for steep slope devices such as TFETs which require less gate voltage than a conventional MOSFET to switch between the on and off state. Small point subthreshold swings (SS) of < 60mV/dec have been demonstrated experimentally by different groups, but it remains challenging to achieve steep slope characteristics over a significantly large switching range. Theoretically it is predicted that vertical device structures based on line tunneling can achieve steeper average switching characteristics and higher on-currents than devices based on pure point tunneling [1-2]. However it has been pointed out that in these devices parasitic diagonal tunneling (point tunneling) has to be circumvented because it may heavily degrade the device performance [3]. It is the goal of this paper to show how to identify the detrimental tunneling contributions in experiment and how to control the gate-voltage-onset with the help of counter doping, resulting in a low average SS.

2. Experimental

Device concept and Fabrication

Starting from 200 mm SOI wafers with 145 nm buried SiO_2 and 10 nm Si, 13 nm B-doped $Si_{0.50}Ge_{0.50}$ followed by a ~7 nm Si cap were grown by RP-CVD. The Si cap layer was grown in an intrinsic and an n-doped variant. Using reactive ion etching, the Si cap was removed everywhere except in the lithographically defined mesa region. A wet etching solution was used to selectively remove the exposed SiGe with respect to Si. By this process an undercut below the Si cap layer is realized. As a consequence the Si cap layer bends towards and finally touches the SOI underneath as seen in Fig. 1. By this means an air bridge isolation is created preventing direct source-drain leakage, therefore decreasing the off-state leakage significantly [3]. After wet chemical cleaning a 5 nm HfO_2/40 nm TiN gate stack (EOT~2 nm) was deposited with ALD/RSD (Reactive Sputter Deposition) covering the complete mesa region including the Si air bridge. The drain contact is formed by P^+-ion implantation into the SOI region around the gate and the dopants are activated by RTA. Subsequently a recess area in the center of the gate is created by removing TiN, HfO_2 and the Si cap layer with selective wet chemistry in order to contact the SiGe layer. From this contact shown on the right in Fig. 1 the current is injected. In the whole overlap area A_{gs} (or overlap length d_{gs} in 2D) line tunneling is expected to occur, with the tunneling path aligned with the electric field of the gate. Additionally parasitic point tunneling along the path indicated by the red arrow in Fig. 1 may take place.

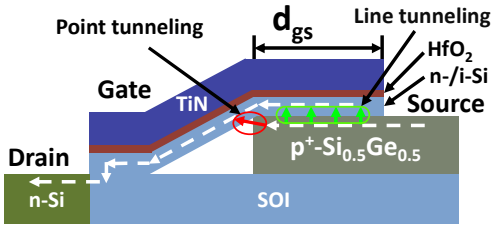

Fig. 1 Device concept with line and point tunneling paths indicated. Drain and source are connected via an air bridge to prevent direct source-drain leakage.

Electrical characterization

Fig 2. shows typical transfer measurements carried out on three types of devices differing in size. A dispersion of the on-current with increasing size becomes apparent in the raw data. By normalizing the data to the gate-source overlap area A_{gs} the dispersion disappears, prompting the relation $I_{on} \propto A_{gs}$. This behavior is in accordance with the theoretical expectations for line tunneling. The simulation in Fig. 3 exhibits the

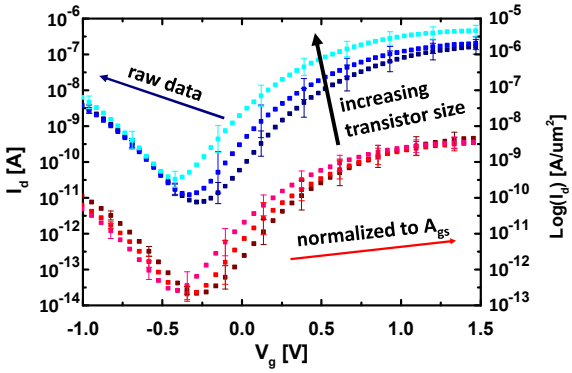

Fig. 2 Transfer characteristics of three transistor types with increasing gate area. Each curve was averaged over 20 devices. The on-current is proportional to the gate-source overlap area A_{gs} and therefore dominated by line tunneling.

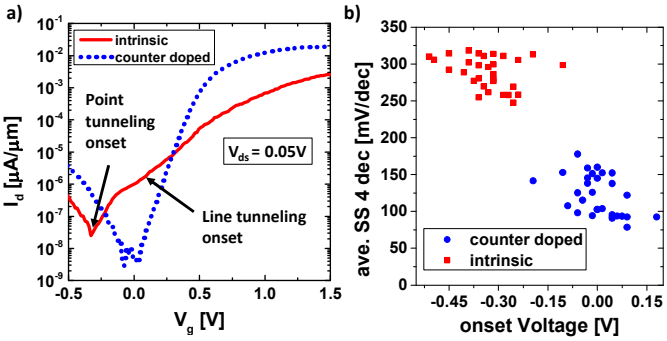

Fig. 4 a) Transfer characteristics of two devices with intrinsic and counter doped channel. On-current, off-current and average slope are much improved due to counter doping. b) A clear correlation between average SS and onset voltage is observed, illustrating the importance of controlling the shift between point and line tunneling.

same trend as in experiment with the on-current increasing by the same factor as the source-gate overlap length (d_{gs}). Therefore line tunneling (see Fig. 1) can clearly be identified as the major contributor to the total current in the on-state of the transistor. However, this does not apply to the subthreshold regime, where point tunneling can play a major role. The transfer curves between 0.2 V and 0.5 V (Fig. 3) overlap because here the current is governed by the parasitic point tunneling path (compare Fig. 1) which is identical for all simulated devices and independent of d_{gs}. Apparently, the transition between point and line tunneling leads to a shoulder in the transfer curve which has severe negative consequences on the average slope. Such a behavior can be reproduced in experiment. The transfer curve labeled as "intrinsic" in Fig. 4(a) exhibits such a shoulder around $V_g = -0.2$ V. It corresponds to a device where the channel is undoped. Our statistics yield that average SS over four orders of I_d do not go far below 250 mV/dec in such devices. However in devices where the channel is moderately counter doped with phosphorous to a level of roughly $3 \cdot 10^{18}$ cm^{-3} this issue is completely resolved. As seen in Fig. 4a) and b) the onset in these devices is shifted by a few hundred mV towards higher voltage. As a consequence no transition or shoulder as seen in Fig. 3 is present over the whole switching range, which results in significantly improved average SS. Fig 4b) emphasis that the reduced SS is strongly correlated with the onset voltage. This correlation reflects the circumstance that the onset of point and line tunneling are closely merged. Furthermore by the use of counter doping the tunneling junction sharpens which leads to an increase in on-current. Simultaneously the off-current is slightly decreased so that the I_{on}/I_{off} ratio exceeds values of 10^6. A comparison of the achieved results is given in table I. EOT scaling is expected to yield further improvements.

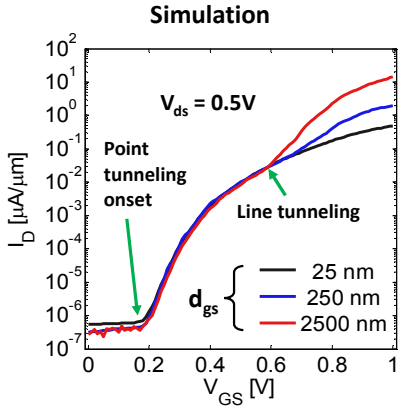

Fig. 3 TCAD simulation for three transistors with increasing gate-source overlap length d_{gs}. The dominant contribution of line tunneling to the total current at $V_g > 0.6$ V can be identified by the d_{gs}-scaling. The early onset is governed by point tunneling, which is independent of d_{gs}.

Table I: Improvement of performance numbers due to counter doping.

	Average I_{on}/I_{off}	Best I_{on}/I_{off}	Best 4 dec SS [mV/dec]
Intrinsic	$3.0 \cdot 10^4$	$5 \cdot 10^4$	247
Counter doped	$1.4 \cdot 10^6$	$4.7 \cdot 10^6$	87

3. Conclusions

We have shown that the key to achieving good performance in vertical TFET structures based on SiGe/Si-heterostructures, especially in terms of average SS, lies in matching the onset voltage of point and line tunneling. This is achieved by means of counter doping, which also boosts the on-current. As expected from theory the on-current was proven to be line tunneling dominated and to scale with the source-gate overlap area A_{gs}.

Acknowledgements

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