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Performance Improvement of Ge-source/Si-channel hetero-junction tunneling FETs: Effects of Annealing Gas and Drain doping Concentration

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Abstract

We examine the effects of gas ambient (N_2 and forming gas (4% H_2/N_2)) and a doping concentration in drain regions on electrical characteristics of Ge/Si hetero-junction tunneling FETs (TFETs). The large on current and steep SS are realized by forming gas PMA and low drain doping concentration, respectively. This improvement is attributable to the reduction in D_{it} in the channel region and in gate-induced drain leakage current in the drain regions.

1. Introduction

A tunneling field-effect transistor (TFET) is one of the most promising concepts for ultra-low power devices, which relies on the band-to-band tunneling mechanism. A Ge/Si hetero-structure with staggered type-II band alignment can effectively reduce the tunneling width in the source junction. Thus, this structure is expected to provide high on/off current ratio and steep subthreshold swing (SS) and some degree of the performance improvement has been demonstrated [1-3]. Furthermore, it has been reported that reduction in D_{it} at MOS interfaces is a critical factor for high performance Ge/Si hetero-junction TFETs [2, 3]. In this study, we examine effects of gas ambient (N_2 and forming gas (4% H_2/N_2)) in post metallization annealing (PMA) and the drain doping concentration on the electrical characteristics of the Ge/Si hetero-junction TFETs for performance improvement.

2. Experiment

Fig. 1 shows the schematic process flow of the Ge/Si hetero-junction TFETs. A 10-nm-thick silicon-on-insulator (SOI) substrate is used for a starting material. Phosphorus ion implantation (I/I) is used for drain formation. Here, one key process is the drain doping concentration optimization. Thus, phosphorus ion dose is varied from 3×10^{14} and 7×10^{14} cm^{-2} to evaluate the effects on the Ge/Si TFET performance. 25-nm-thick in situ boron-doped Ge layers are grown at 150 ^oC by molecular beam epitaxy (MBE). 2-step 3.4-nm-thick Al_2O_3 is formed by atomic layer deposition with electron cyclotron resonance (ECR) plasma post oxidation to ensure the high quality MOS interface between Al_2O_3 and Ge [4]. Ta is deposited as the gate metal, followed by Ni and Al deposition for the source contact and the contact pad, respectively. Lastly, PMA is carried out at 400 ^oC in N_2 or forming gas (4% H_2/N_2) for 30 minutes.

3. Results and Discussion

Fig. 2 (a) and (b) show the drain current-gate voltage (I_D-V_G) and drain current-drain voltage (I_D-V_D) characteristics of the fabricated devices, respectively. It is found that the electrical properties of the Ge/Si TFETs such as I_{on} and SS are better in the forming gas PMA than in the N_2 one ambient. The averaged SS (SS_{avr}) close to the thermal limit (60 mV/dec.) and large I_{on}/I_{off} over 7 orders are obtained after PMA, as shown in Fig. 3. Here, SS_{avr} are defined as the SS values averaged over 3 decades of I_D from the minimum I_D. The temperature dependence of the I_D-V_G characteristics is measured at temperature from 300 to 150 K (Fig. 4), in order to confirm the mechanism of the current of the present devices. I_{on} in the high V_G region and SS values are almost independent of temperature. I_D of the fabricated devices is also independent of the gate length (Fig. 5). These results indicate that the current is dominated by band-to-band tunneling (BTBT) occurring near the Ge/Si junctions [5].

Fig. 6 shows the energy distributions of interface state density (D_{it}) between Si and Al_2O_3-gate insulator. Forming gas PMA without PDA produces the relatively low D_{it} at the Al_2O_3/n-Si interface of 2×10^{11} $eV^{-1}cm^{-2}$, suggesting the effective hydrogen passivation with the Al_2O_3/Si interface. As a result, improvement of the TFET performance by forming gas PMA is attributable to this reduction in D_{it}.

Meanwhile, the drain doping concentration is another critical factor. The high doping concentration can increase the tunneling probability near drain side in the off condition, as illustrated in Fig. 7, which causes degradation of the TFET characteristics. On the other hand, a too low doping concentration can decrease I_{on} through high contact resistance. For this reason, optimization of the drain doping concentration is required. Fig. 8 (a) and (b) show the I_D-V_G and the SS-I_D characteristics, respectively, as a parameter of the drain I/I dose. I_{off} and SS of the Ge/Si TFETs are more improved for lower I/I dose, because of the decrease of tunneling current near drain side. Fig. 9 (a) summarizes I_{on}, I_{off} and I_{on}/I_{off} ratio variation as a function of the drain I/I dose. As the I/I dose decreases, I_{off} decreases with maintaining constant I_{on}, leading to the increase in the I_{on}/I_{off} ratio. Furthermore, gate-induced drain leakage (GIDL) ratio is reduced in lower I/I dose, as shown in Fig. 9 (b). These results mean that the doping concentration of the drain regions in TFETs is also a critical factor for TFET performance.

4. Conclusions

The impacts of gas ambient and the doping concentrations in drain regions on the electrical characteristics of Ge/Si hetero-junction TFETs were experimentally studied. The higher TFET performance with higher I_{on} and steeper SS was realized by forming gas (4% H_2/N_2) PMA. Furthermore, lower SS values and lower I_{off} were obtained for lower P I/I dose in the drain regions. It was revealed that D_{it} in the channel region and GIDL determined by the doping concentration in drain regions are critical factors for realizing high performance Ge/Si hetero-junction TFETs.

Acknowledgements

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References

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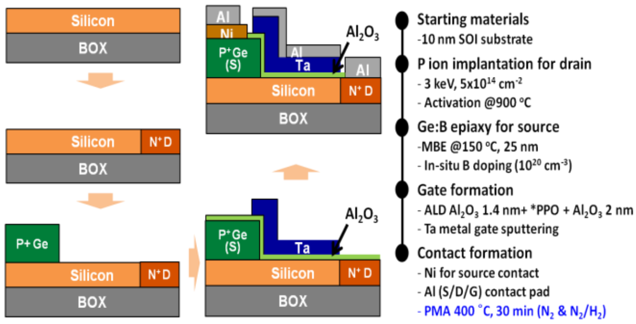


Fig. 1 Schematic process flow of the Ge/Si heterojunction TFETs.

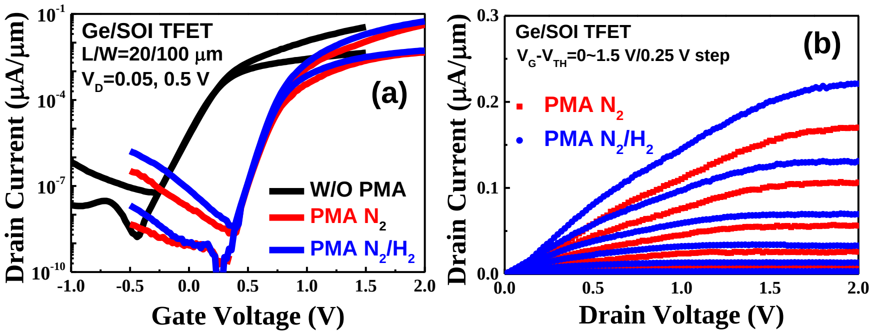


Fig. 2 (a) I_D-V_G and (b) I_D-V_D characteristics of the fabricated devices.

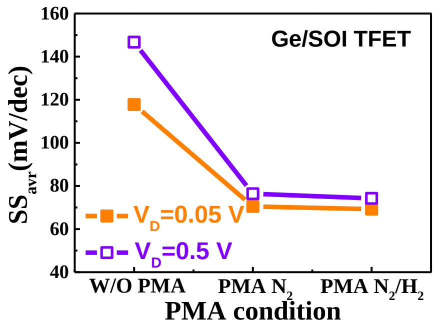


Fig. 3 SS_{avr} in different annealing conditions.

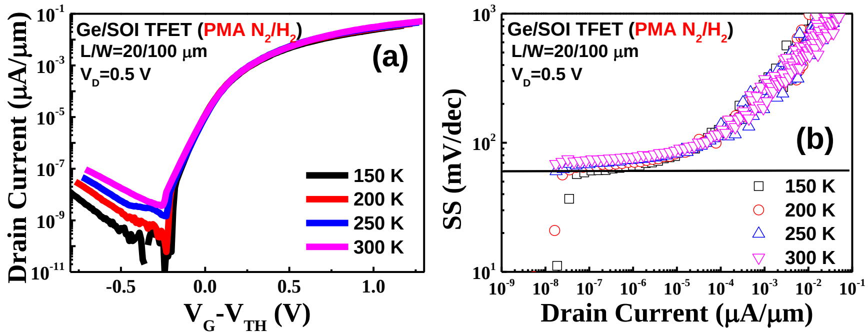


Fig. 4 (a) I_D-V_G and (b) SS-I_D characteristics depending on temperature.

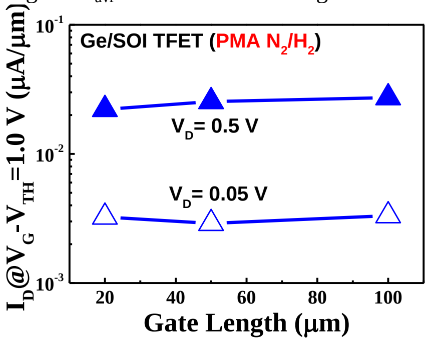


Fig. 5 Gate length dependency of Ge/Si TFETs.

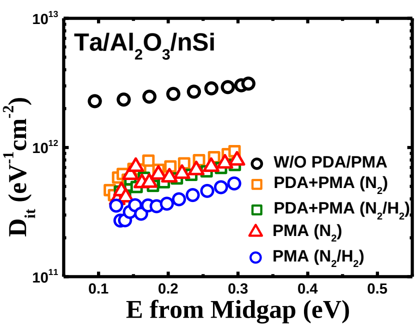
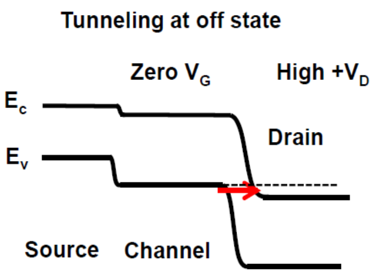


Fig. 6 D_{it} in the Al_2O_3/nSi interface with different annealing conditions.



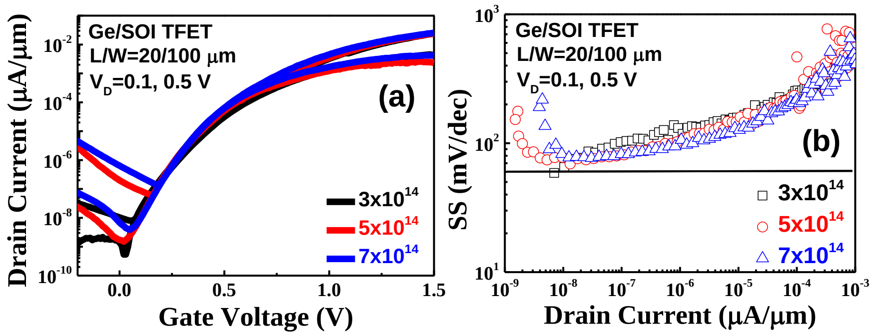


Fig. 8 (a) I_D-V_G and (b) SS-I_D characteristics with different drain ion dose concentration.

Fig. 7 Band structure of TFET with high doping concentration in drain region.

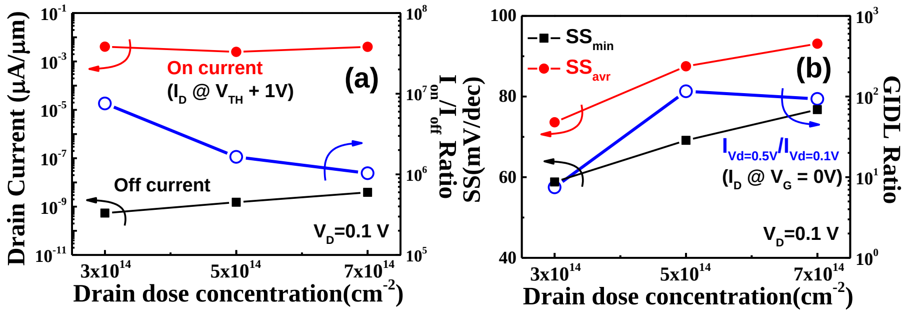


Fig. 9 (a) I_{on}, I_{off} and I_{on}/I_{off} ratio and (b) SS and GIDL ratio with different drain ion dose concentration.