Extended Abstracts of the 2017 International Conference on Solid State Devices and Materials, Sendai, 2017, pp237-238

E-4-03

Fringing Field Effects in Ferroelectric Negative Capacitance Field-Effect Transistors

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We study the role of the gate fringing field in ferroelectric negative capacitance (NC) transistors using technology computer-aided design simulation. The fringing field on the drain side enhances NC's function of desirably modulating the effective gate voltage and improves subthreshold swings of such transistors, which effect becomes stronger with increasing drain voltage or decreasing gate length.

1. Introduction

Semiconductor integrated circuits (ICs) are required to be low-power for mobile, wearable, and Internet-of-Things applications. An effective way of reducing ICs' energy consumption is to lower the power supply voltage V_{DD}. To do this, transistors used in ICs should be turned on and off steeply within a narrow input voltage range. The switching steepness is measured by the subthreshold swing S, which is defined as the gate voltage width required to vary the drain current I_D by an order of magnitude in the subthreshold region. The smaller S transistors have, the lower V_{DD} their ICs can operate with. However, the S of standard metal–oxide–semiconductor (MOS) field-effect transistors (FETs) has a physical lower limit of about 60 mV/dec at room temperature. Various transistors whose operating principle differs from that of standard MOS FETs have been proposed to overcome this limit. One is tunnel FETs [1], which drive a current based on the band-to-band tunneling of electrons. Another example is negative capacitance (NC) FETs having a ferroelectric layer in the gate stack [2], which operate similarly to standard MOS FETs except that the ferroelectric layer helps the gate voltage control the channel potential. They are currently being intensively investigated and several demonstrations of steep switching with an S less than 60 mV/dec have already been reported [3–5]. Not only experimental but also simulation and modeling studies on the NC FETs are active for the understanding of the device physics, prediction of the behavior, and exploration of proper device structures and ferroelectric materials [6–13]. In most of these studies, the considered device structure does not have gate sidewalls (SWs) and consequently the gate fringing field is ignored. We have predicted that decreasing gate length L_G improves the subthreshold characteristics of NC Fin FETs and pointed out the possibility that the fringing field plays an important role in creating this interesting trend [13]. In this study, we thoroughly analyze the effects of the fringing field on the performance of ferroelectric NC FETs using technology computer-aided design (TCAD) simulation.

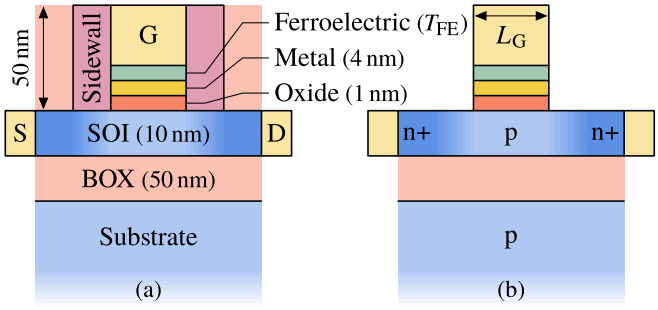

Fig. 1. Schematic views of the considered ferroelectric NC SOI FETs (a) with and (b) without SWs. The thicknesses of some thin-film components are shown in parentheses in their labels.

2. Simulation Framework

We considered NC silicon-on-insulator (SOI) FETs having a metal–ferroelectric–MOS (MFMOS) structure, illustrated in Fig. 1(a). The internal metal layer between the ferroelectric and oxide layers is expected to stabilize the NC state of the ferroelectric layer by uniforming the electric field applied to the layer [6, 14]. The electrostaic potential $\phi(\boldsymbol{r})$ in an electronic device is generally described by Poisson's equation,

$$\nabla \cdot [-\varepsilon(\boldsymbol{r})\varepsilon_0 \nabla\phi(\boldsymbol{r})] = \rho(\boldsymbol{r}), \quad (1)$$

where $\varepsilon(\boldsymbol{r})$ is the dielectric constant, ε_0 is the permittivity of vacuum, and $\rho(\boldsymbol{r})$ is the charge density. In a typical TCAD simulation, this equation is solved simultaneously with the current continuity equations of electrons and holes in the semiconductor regions of the device by iterative calculations based on the Newton–Raphson method. Equation (1) uses an assumption that the polarization $\boldsymbol{P}$ in a material is proportional to the applied electric field $\boldsymbol{E}$. However, the $\boldsymbol{P}$–$\boldsymbol{E}$ relationship in a ferroelectric material is complicated as shown in Fig. 2(a). Although the relationship shown by the dotted line is well-known, under a specific condition, that shown by the solid line can be realized. It should be noted that, on the line of A–B, the ferroelectric material is in a NC state and has a negative permittivity as shown in Fig. 2(b). The $\boldsymbol{P}$–$\boldsymbol{E}$ relationship passing through the NC state is given by [2]

$$2\alpha|\boldsymbol{P}| + 4\beta|\boldsymbol{P}|^3 + 6\gamma|\boldsymbol{P}|^5 = |\boldsymbol{E}|, \quad (2)$$

where α (= −1.54 Gm/F), β (= −2.65 Tm^5/FC^2), and γ (= 2.60 Pm^9/FC^4) are the material parameters. In our simulation, we calculated $\boldsymbol{P}$ in the ferroelectric layer from this equation with an assumption that $\boldsymbol{P}$ is parallel to $\boldsymbol{E}$ at every iteration, and solved the following equation instead of Eq. (1) for the layer:

$$\nabla \cdot [-\varepsilon_0 \nabla\phi(\boldsymbol{r}) + \boldsymbol{P}(\boldsymbol{r})] = \rho(\boldsymbol{r}). \quad (3)$$

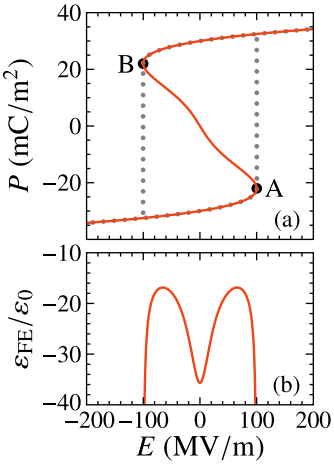

Fig. 2. (a) Polarization of the considered ferroelectric material plotted as a function of the external electric field. The material is in a NC state on the line of A–B. (b) Permittivity of the material in the NC state.

3. Results and Discussion

Figure 3(a) shows the I_D vs gate-to-source voltage V_{GS} characteristic of the NC FET with L_G of 40 nm and the ferroelectric layer thickness T_{FE} of 5 nm shown in Fig. 1(a) at the drain-to-source voltage V_{DS} of 0.05 V. The open circle represents the

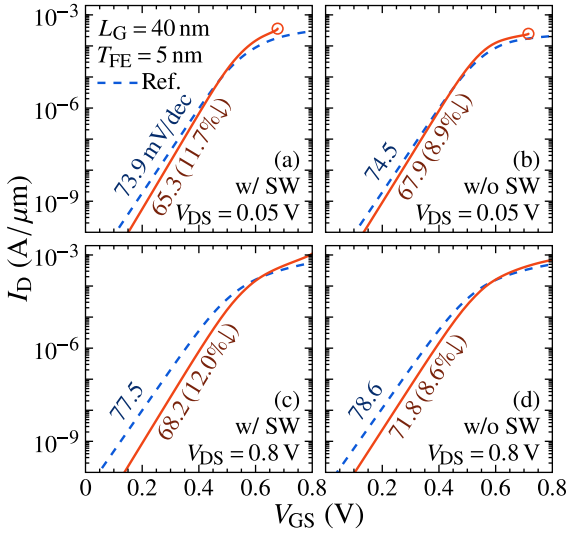

Fig. 3. [(a) and (b)] I_D–V_{GS} characteristics of NC FETs with and without SWs at V_{DS} of 0.05 V. The results obtained for standard MOS FETs are also shown by the dashed lines. [(c) and (d)] Same plots as in (a) and (b) but for V_{DS} of 0.8 V.

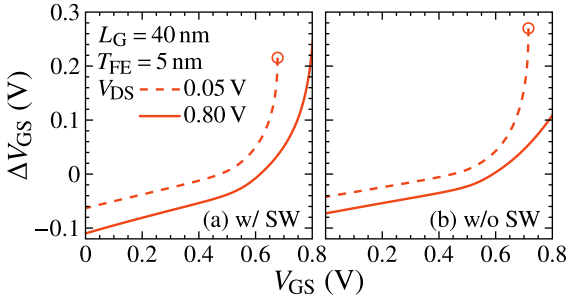

Fig. 4. Voltages applied to the ferroelectric layers ΔV_{GS}'s of NC FETs (a) with and (b) without SWs plotted as a function of V_{GS}. A voltage of V_{GS} + ΔV_{GS} is applied to the MOS structure beneath the layer.

state where the gate capacitance falls to zero and the simulation was terminated. The figure also shows the I_D–V_{GS} characteristic of the corresponding MOS FET. Comparing the two characteristics, we can see that the NC improves the subthreshold characteristic of the NC FET. This is because the ferroelectric layer modulates V_{GS} to decrease I_D in the subthreshold region as shown in Fig. 4(a) by the dashed line. Note that the layer always helps V_{GS} bend the band in the channel region regardless of the bending direction and starts to increase I_D through the V_{GS} modulation when V_{GS} surpasses the flat-band voltage. Figure 3(b) shows the I_D–V_{GS} characteristic of the NC FET without SWs shown in Fig. 1(b). Although the NC improves S similarly to the case in the NC FET with SWs, the improvement is smaller because the V_{GS} drop across the ferroelectric layer is smaller as can be seen by comparing the dashed lines in Figs. 4(b) and 4(a). The SWs allow electric force lines from

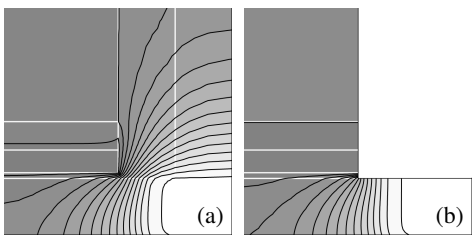

Fig. 5. Potential distributions in NC FETs (a) with and (b) without SWs at V_{GS} of 0 V and V_{DS} of 0.05 V.

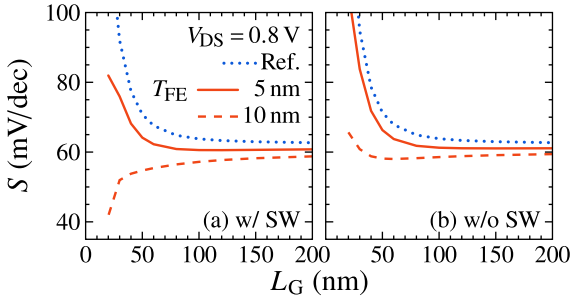

Fig. 6. L_G dependence of S of NC FETs (a) with and (b) without SWs.

donor ions in the drain to reach the internal metal as shown in Fig. 5(a) and then positive charges are induced on the internal metal surface facing the ferroelectric layer, which strengthens the electric field applied to the ferroelectric layer and hence the polarization. As a result, the V_{GS} drop increases. This effect caused by the gate fringing field near the drain should be stronger with increasing V_{DS}. Figures 3(c) and 3(d) show the I_D–V_{GS} characteristics of the NC FETs with and without SWs at V_{DS} of 0.8 V. The difference between improvements in S in the two NC FETs becomes somewhat larger compared with the case for V_{DS} of 0.05 V. This is because increasing V_{DS} enhances the fringing field effect and further increases the V_{GS} drop as seen in Fig. 4. Note that, because of an increase in the leakage current through the bottom of the SOI layer, S at V_{DS} of 0.8 V is worse than that at V_{DS} of 0.05 V for both NC FETs. Figures 6(a) and 6(b) show S of the NC FETs with and without SWs as a function of L_G. With decreasing L_G, the fringing field effect becomes larger and accordingly the difference in S for the two NC FETs also becomes larger. The figures also show the results obtained when T_{FE} is 10 nm. In this situation, the L_G dependence of S is quite different between the two NC FETs. As can be clearly seen from this fact, the fringing field has a significant impact on the behavior of NC FETs.

4. Conclusion

We have studied the effects of the gate fringing field on the performance of NC FETs with an MFMOS structure in TCAD simulation. The fringing field near the drain enhances the NC function of desirably modulating the effective gate voltage, which improves the performance in the subthreshold region. These effects become stronger with increasing drain voltage or decreasing gate length and therefore the fringing field should be taken into account for accurate and precise simulation and modeling of the NC FETs, especially of the scaled ones.

Acknowledgment—This work was partially supported by CREST, JST Grant No. JPMJCR14F2.

References

[1] W. Y. Choi *et al.*, IEEE Electron Device Lett. **28**, 743 (2007).
[2] S. Salahuddin and S. Datta, Nano Lett. **8**, 405 (2008).
[3] A. Rusu *et al.*, IEDM Tech. Dig., 2010, p. 395.
[4] S. Dasgupta *et al.*, IEEE J. Explor. Solid-State Comput. Device Circuits **1**, 43 (2015).
[5] J. Jo and C. Shin, IEEE Electron Device Lett. **37**, 245 (2016).
[6] A. I. Khan *et al.*, IEDM Tech. Dig., 2011, p. 255.
[7] H. Ota *et al.*, Jpn. J. Appl. Phys. **55**, 08PD01 (2016).
[8] H. Ota *et al.*, Jpn. J. Appl. Phys. **56**, 04CD10 (2017).
[9] D. Jiménez *et al.*, IEEE Trans. Electron Devices **57**, 2405 (2010).
[10] C. Jiang *et al.*, J. Phys. D: Appl. Phys. **48**, 365103 (2015).
[11] C. Jiang *et al.*, Jpn. J. Appl. Phys. **55**, 024201 (2016).
[12] G. Pahwa *et al.*, IEEE Trans. Electron Devices **64**, 1366 (2017).
[13] H. Ota *et al.*, IEDM Tech. Dig., 2016, p. 318.
[14] S. Kasamatsu *et al.*, Adv. Mater. **28**, 335 (2016).