Extended Abstracts of the 2017 International Conference on Solid State Devices and Materials, Sendai, 2017, pp239-240

E-5-01 (Invited)

Improvement of Device and Circuit Performance of Si-based Tunnel Field-Effect Transistors by Utilizing Isoelectronic Trap Technology

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Abstract

Tunnel field-effect transistor (TFET) is one of the candidates replacing conventional MOSFETs to improve the power efficiency of LSIs. The most significant issue concerns their low tunneling current. Si is an indirect gap material having a low tunneling probability and is not favored for the channel of TFETs. Then, we proposed and demonstrated the performance improvement of Si-TFETs in device and circuit level utilizing the isoelectronic trap (IET) technology to enhance tunneling probability. IET technology paves a way to realize practicable I_{ON} in TFETs with Si technologies.

1. Introduction

Now we are at the last stage of miniaturization of MOSFETs. However, the enhancement of computing performance is still demand. It was pointed out that the improvement of power efficiency is essential for that of computing performance [1]. Then, we have to continue to improve the power efficiency of LSIs. The power consumption of transistors is a significant issue, and steep slope devices such as tunnel field-effect transistors (TFETs) has been attracted.

TFETs are a kind of gated p-i-n diodes. The gate regulates tunneling current flowing through a pn junction, which enables TFETs to realize steeper switching than that of MOSFETs. The low ON current (I_{ON}) is the most significant issue in TFET research. Because the tunneling current is essentially related to material properties, many TFETs with new materials, including not only Ge or III-V materials [2] but also two-dimensional semiconductors [3], have been reported. Si is not favored because of its low tunneling probability resulting from its indirect-gap material nature (Fig. 1).

Recently, we have proposed and demonstrated a technique to enhance tunneling probability in Si, which utilizes isoelectronic traps (IETs) [4-7]. The IET technology provides a new approach to realize high I_{ON} in TFETs. In this presentation, we discuss performance improvement of complementary TFETs in device and circuit level thanks to the IET technology.

2. Isoelectronic Trap(IET) technology

IET technology is to produce an intermediate isolated state in the pn junction and utilizes the tunneling current mediated by the state (Fig. 2). The intermediate state acts as a "stepping stone" for electrons tunneling from the valence to conduction bands. In this situation, the intermediate state is not selective regarding wave numbers, like atoms. Following this scenario, we can aim to relax the k-conservation rule in indirect-gap semiconductors and realize pseudo-direct tunneling to obtain a higher tunneling rate. Here, isoelectronic impurities (IEIs) are chosen to form the intermediate state. Specifically, the Al-N pair is chosen as IEIs in our work (Fig. 3). The theoretical view of IET-assisted tunneling (IETT) has been provided by Iizuka et al. in detail [8].

3. Experimental Demonstration

We demonstrated the benefit of IET technology in TFETs with not only single devices [4] but also circuits [6]. Through these works, we utilized TFETs fabricated on SOI wafers. Firstly, we show one example for single device demonstrations, for which Figs. 4 shows I_D–V_D curves of the control- and IET-TFETs [6]. The IET produced higher current in both P- and N-TFETs thanks to IETT. The enhancement was five times for P-TFETs and two times for N-TFETs. It is noted that the enhancement ratio was lower than our other works [4] because we performed different fabrication process. Furthermore, the first proof-of-concept experiment using diodes exhibited 735 times enhancement of tunneling current [4]; therefore, it promises that much better current enhancement also in TFETs.

Next, we show two demonstrations with circuits. Frist one is complementary TFET inverters (Fig. 5). The inverters with the IET-TFETs exhibited steeper transition, especially in the lower V_{DD} range, thanks to the I_{ON} enhancement. The non-ideal curve features resulted from the ambipolarity of the TFETs. The inverter with the IET-TFETs exhibited a better voltage gain than that for the control in the entire V_{DD} range. The transconductance improvement due to the I_{ON} enhancement by the IET technology is attributed to the improved voltage gain. Another is Complementary TFET ring oscillators (ROs) (Fig. 6). Note that this was the first demonstration of the TFET-RO operation. The IET technology also improved the RO operation, in which a higher output frequency was realized thanks to the IET technology.

3. Summary

We have proposed and demonstrated a technique to improve TFET circuit performance utilizing IETs. IET technology opens the door to realize I_{ON} enhancement in Si-TFETs, which enables Si-TFETs to compete with new-materials-based TFETs. Si technology has an advantage in the ease of integration and cost. Promisingly, much higher I_{ON} enhancement was theoretically predicted with realizing steeper pn junction [8]. IET technology paves a way to realize TFET-based LSIs with low power consumption with Si technology.

Acknowledgements

This study was partially based on results obtained from a project commissioned by the New Energy and Industrial Technology Development Organization (NEDO), Japan. This study was also supported by JSPS KAKENHI Grant-in-Aid for Young Scientists (A) No. 15H05526. The authors thank Prof. Nakayama and Dr. Iizuka for their insightful comments on this work.

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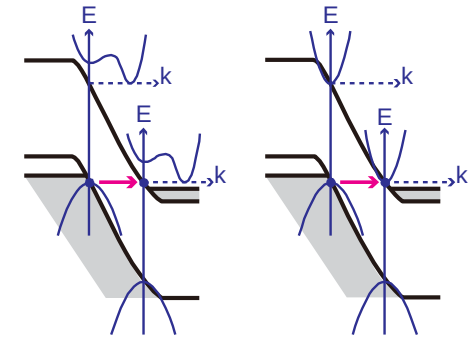

Fig. 1. Schematic views of indirect and direct processes for Zener tunneling. The E–k relationship is superimposed on band diagrams.

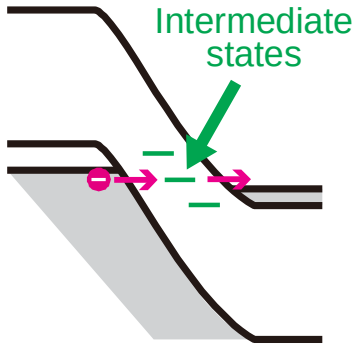

Fig. 2. Schematic showing the idea of using intermediate states for tunneling through a pn junction.

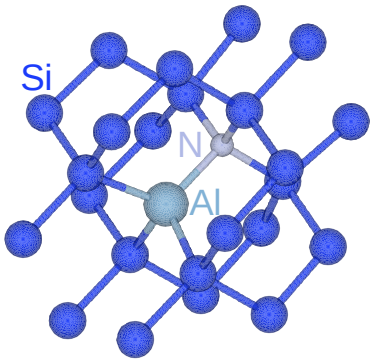

Fig. 3. Schematic atomic configuration of an Al–N pair in a host Si crystal [9, 10].

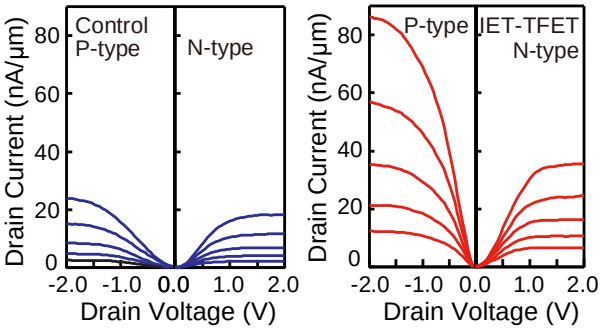

Fig. 4. I_D–V_D curves of the control and IET-TFETs [6]. V_G was varied in the $|V_G-V_{TH}|$ range of 0.6–1.0 V. IET technology improves the tunneling current. The higher I_D in IET-TFETs results from probability enhancement.

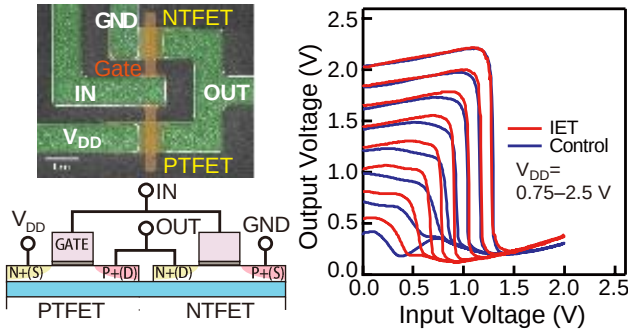

Fig. 5. (Left) SEM picture and schematic circuit of the TFET inverter. The source of the P-type is connected to V_{DD}, and the source of the N-type to GND. (Right) Transfer curves of TFET inverters [6]. The inverter with IET-TFETs exhibited steeper curves.

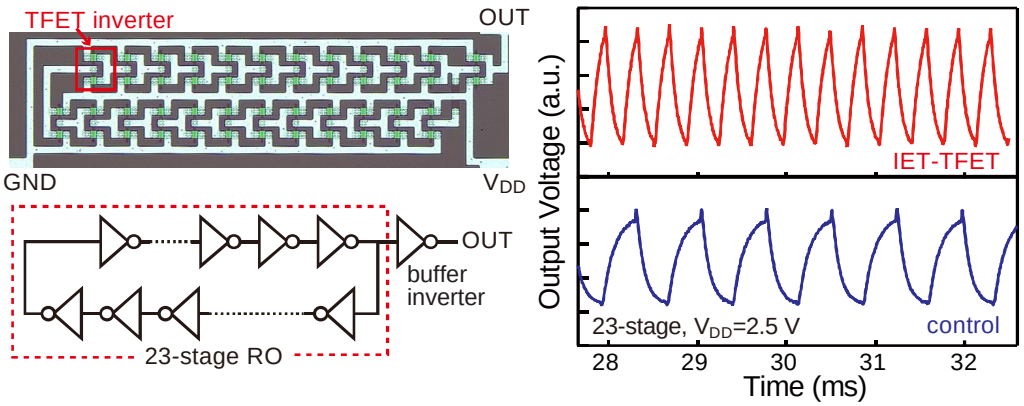

Fig. 6. (Left) Optical microscope image and schematic circuit diagram of the fabricated 23-stage ring oscillator (RO). All transistors are TFETs. (Right) Output waveforms of the ROs [6]. The IET-TFET RO exhibited a higher frequency than the control.