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Investigation of Thermal Effects on FinFETs in the Quasi-ballistic Regime

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Abstract

In this paper, the thermal effects of FinFETs in quasi-ballistic regime are investigated using Monte Carlo method. The bulk Si nFinFETs with the same fin structure and two different gate lengths 20nm and 80nm are investigated and compared to evaluate the thermal effects on the performance of FinFETs especially in the quasi-ballistic regime. The ON currents of the 20nm FinFET with V_{gs}=0.7V will not decrease with the increasing lattice temperature (T_L) at high V_{ds} and even has 0.76% ON current increment at V_{ds}=0.7V and 400K. The V_{th} in 20nm FinFET is more affected by T_L than in 80nm FinFET. But T_L less affects the electron transport in 20nm FinFET. The thermal effects in quasi-ballistic regime show a different way, which should be considered in the device modeling and design.

1. Introduction

As transistors advance into nanoscale, thermal effects become noteworthy. Lattice temperature (T_L) has effects on both electrostatic properties and carrier transports. In electrostatic properties, high T_L can shorten the bandgap width and increase the effective density of states, which will lead to increased carrier density. In carrier transports, high T_L can lead to larger electro/hole-phonon scatterings, which will lead to the carrier velocity degradation. Due to these effects, the device performance can be significantly affected by T_L. Some works [1~2] have studied the effects and most of them found that the thermal effects could lead to on-current degradation. However, most of the results were obtained with large operating voltages or within large-scale devices. In nano-scale devices, carrier transport has become quasi-ballistic [3]. There will be less scattering events occurred. What's more, threshold voltage of transistors doesn't scale down as the operating voltage V_{dd} [4], which leads to smaller overdrive voltage so that the electrostatic properties become more sensitive to T_L changes. In this paper, we will compare device performances in bulk Si nFinFETs with two different gate lengths 20nm and 80nm to investigate the thermal effects in the quasi-ballistic regime.

2. Simulation method and device structure

The in-house 3D full-band ensemble Monte Carlo simulator [5] is utilized in this work. Full band structure of silicon is employed, which is obtained from empirical pseudopotential calculation including spin-orbit interactions. Acoustic and optical phonon scattering, ionized impurity scattering, surface roughness scattering and impact ionization are included. The impacts of different lattice temperatures on carrier distributions, phonon distributions, bandgap width and scattering rates are considered so that the thermal effects can be included in this simulator. Three different lattice temperatures T_L=300K, 360K and 400K are considered to study the thermal effects. The bulk Si nFinFETs [6] are simulated with different gate lengths in this work, whose structure is shown in Fig.1 and the structure parameters listed in Table I. Fig.2 shows the simulated and experimental I_{ds}-V_{ds} curves of 20nm FinFET, and it can be seen that the MC simulation results can well reproduce the experimental data only by changing the surface roughness scattering.

3. Results and Discussions

Fig. 3 shows the I_{ds}-V_{ds} characteristics of the 20nm FinFET and the 80nm FinFET at V_{gs}= 0.7V under T_L=300K, 360K, 400K. The inset figures show the degradation rate at 360K and 400K comparing with at 300K, which can be calculated as $(I_{ds}(T_L)-I_{ds}(300K))/I_{ds}(300K)$. By comparing Fig.3(a) and (b), we can find that the ON currents of 80nm FinFET (b) decrease with the increasing of T_L under V_{ds} changing from 0.1V to 1.5V, and the highest degradation is -13% at V_{ds}=0.1V and T_L=400K. But the ON currents of 20nm FinFET (a) will not decrease with the increasing of T_L when V_{ds} changing from 0.5V to 0.7V and even have 0.76% ON current increment at V_{ds}=0.7V and T_L=400K. To understand the reasons of this phenomenon, two factors, which impacted by the thermal effects, are discussed. First is the charge density. From Fig.4 we can see that increased T_L will lead to charge increasing on the top of source to channel barrier. Fig. 5 shows that increased T_L can significantly lower the V_{th}, and then it will lead to the increased overdrive voltage (V_g-V_{th}). The V_{th} in 20nm FinFET is more sensitive to T_L than that in 80nm FinFET. The reduction of V_{th} can even be 40% at T_L=400K in 20nm FinFET. Second is the carrier transport. The phonon scattering rates of the three temperature conditions are shown in Fig. 6(a). And Fig.6(b) shows the phonon scattering rate degradation rate of 360K and 400K comparing with 300K, which can be expressed as $(S(T_L)-S(300K))/S(300K)$. Fig.7 plots the average velocity distribution along the transport direction, which clearly shows the degradation in velocity due to the high T_L. Fig. 8 shows the injection velocity under different drain voltages and T_Ls. The injection velocity is less affected by T_L in high V_{ds} than in low V_{ds}. Fig. 9 shows the degradation to injection velocities and peak velocities by high T_L in both devices. It shows that the transport in 20nm FinFET is less affected by temperature, which is the result of reduced scattering opportunities. And hence, the ON current doesn't degrade with T_L increasing at high V_{ds}.

4. Conclusions

We investigate the thermal effects of FinFETs in quasi-ballistic regime. The ON currents of the 20nm FinFET with V_{gs}=0.7V will not decrease with the increasing of T_L at high V_{ds} situation and have an 0.76% ON current increment at V_{ds}=0.7V and 400K. The V_{th} is more affected by T_L while the transport is less affected by T_L in 20nm FinFET than in 80nm FinFET. The thermal effects in quasi-ballistic regime show a different way and they should be considered in device modeling and design.

Acknowledgements

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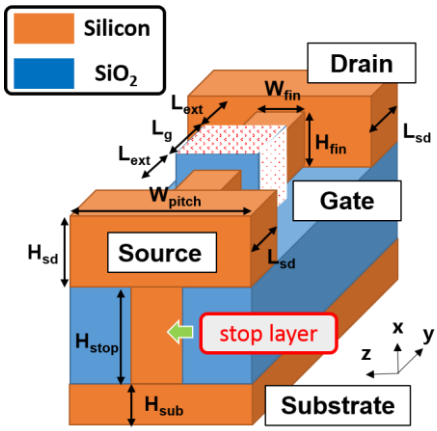


Fig.1 Schematic structure of the bulk Si nFinFET.

Table I Structure parameters of the simulated FinFET

Structure Parameter	Value
Raised S/D height, H_{sd}	52nm
Stop layer height,H_{stop}	40nm
Substrate layer height,H_{sub}	40nm
Fin Height,H_{fin}	42nm
Raised S/D length,L_{sd}	20nm
S/D Extension length,L_{ext}	10nm
Gate length,L_g	20/80nm
Pitch,W_{pitch}	42nm
Fin width,W_{fin}	8nm
Channel doping, n type	$1*10^{15}cm^{-3}$
Stop layer doping, n type	$1*10^{18}cm^{-3}$
Source/Drain doping, p type	$1*10^{20}cm^{-3}$
Gate oxide thickness (EOT)	0.85nm

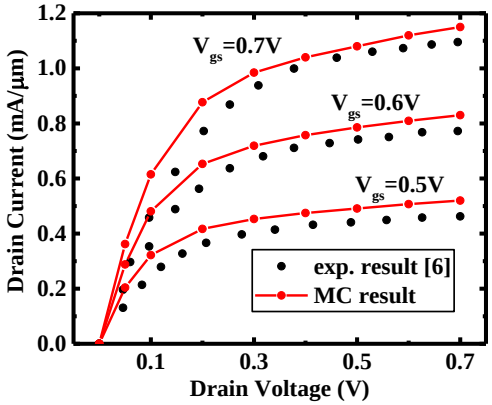
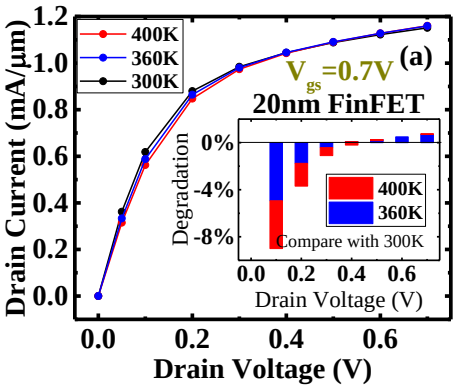


Fig.2 Calibration of 20nm bulk Si nFinFET with experimental data[6].



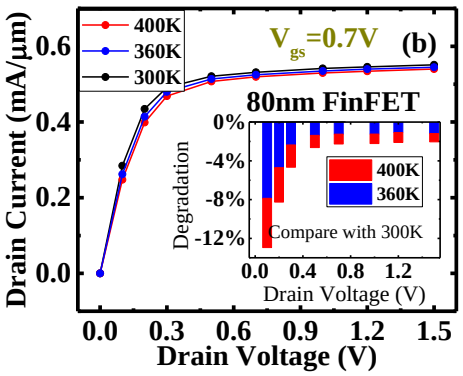


Fig.3(a) I_{ds}-V_{ds} characteristics of 20nm FinFET with T_L=300K, 360K ,400K. Inset figure: Current degradation rate at T_L=360K,400K comparing with that at T_L=300K (b) I_{ds}-V_{ds} characteristics of 80nm FinFET with T_L=300K, 360K ,400K. Inset figure: Current degradation rate at T_L=360K,400K comparing with that at T_L=300K.

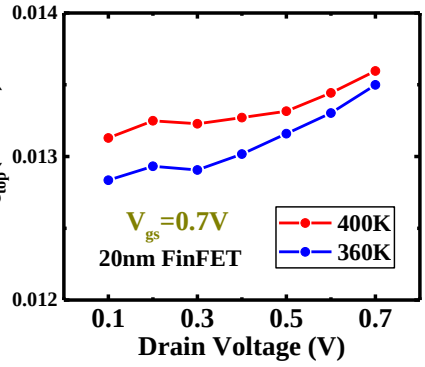


Fig.4 The relationship of the sheet density of electron charge at the top of the source to channel barrier with drain voltage.

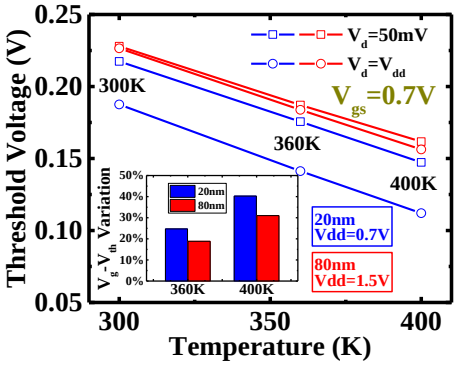


Fig.5 The relationships of threshold voltage with temperature in 20nm FinFET and 80nm FinFET. Inset figure: overdrive voltage variation at 360K and 400K comparing with that at 300K.

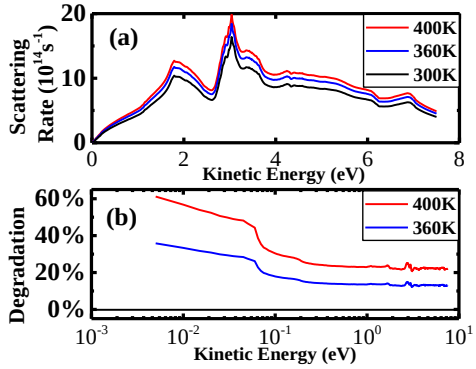


Fig.6(a) electro-phonon scattering rates at T_L=300K,360K,400K. (b) scattering rate degradation percentages at T_L=360K, 400K comparing with that at T_L=300K.

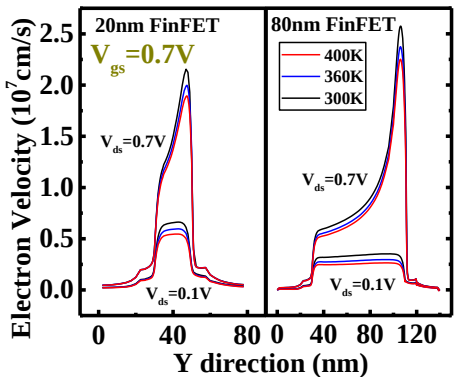


Fig.7 Average velocity distributions along the transport direction in 20nm FinFET and 80nm FinFET.

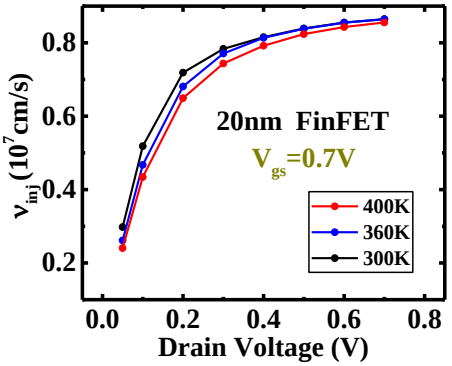


Fig.8 The relationship of the injection velocity at the top of the source to channel barrier with drain voltage.

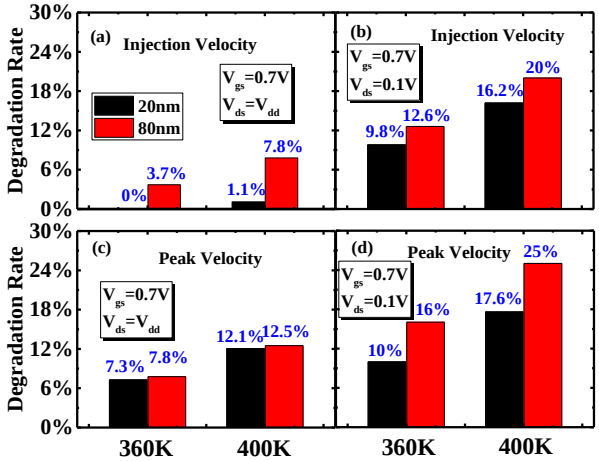


Fig.9 Comparison of the degradation rates of (a) injection velocity at V_{ds}=V_{dd}, (b) injection velocity at V_{ds} =0.1V, (c) peak velocity at V_{ds}=V_{dd} and (d) peak velocity at V_{ds}=0.1V in 20nm FinFET and 80 nm FinFET at T_L=360K,400K. The velocity degradation in low drain voltage situation is larger than that in high drain voltage situation.