Optimizing MOS-Gated Thyristor using Voltage-based Equivalent Circuit Model for Designing Steep Subthreshold Slope PN-Body Tied SOI FET

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Abstract

We proposed a new circuit model that provides a guide on designing MOS-Gated Thyristor (MGT). The impact of design parameters on MGT is examined to find out how to regulate the voltage response of MGT. The model will be useful for designing an SOI MOSFET merged with MGT (i.e., PN-Body Tied SOI FET [1-3]), which shows extremely steep subthreshold slope with very low supply voltage.

1. Introduction

PN-Body Tied SOI FET (PNBTFET) is an SOI MOSFET whose body is attached to the body terminal via a PNP diode (Fig. 1). It shows extremely steep subthreshold slope (SS) less than 6 mV/decade even with a very low drain voltage of 0.1 V [1-3]. Between the source and body terminals is a PNPN structure with a MOS gate, i.e., MOS-Gated Thyristor (MGT) [4] (Fig. 2), whose cathode and anode correspond to the source and body terminals, respectively. It is believed that, when MGT turns on, holes suddenly accumulate in the P body region, causing abrupt increase of the drain current, and steep SS. Therefore, to achieve a PNBTFET with low on and off gate voltages $(V_{on} \text{ and } V_{off})$ with small hysteresis, proper designing of the inherent MGT switching behavior is essential. It should also be noted that, to achieve low power CMOS using PNBTFETs, reduction of the on-state body current I_B is important; the current flowing to the source terminal cannot not be blocked by the series off-state complementary FET, and causes additional standby power dissipation.

Recently, we proposed a new equivalent circuit model of MGT (Fig. 3) [5], which explains the switching mechanism of MGT, and would be useful for exploring such design goals. In this paper, it is demonstrated that the model shows good correlation with the MGT operation, and can be conveniently used for designing PNBTFETs with suitable threshold voltages and low body current.

2. Voltage-based Equivalent Circuit Model

The circuit model in Fig. 3 consists of two cross-coupled voltage inverters, namely, Electron Current Inverter (ECI) and Hole Current Inverter (HCI) [5]. V_P , V_N , and V_G correspond to P region potential, N region potential, and gate voltage, respec-tively. ECI has input V_P and V_G and output V_N , and HCI has input V_N and output V_P . ECI input V_P follows HCI output, and HCI input V_N follows ECI output. In this model, the operating point of V_P and V_N settles at one of the stable points, which are located at the intersection of ECI and HCI transfer curves on V_P - V_N diagram (Fig. 4). Note that upper left stable point indicates off-state, and lower right one on-state. When an off-state stable point disappears as ECI curve is modulated by raising V_G , the operating point in off-state is forced to move instantly to the on-state stable point. In this way, the proposed model can explain the abrupt switching behavior. ECI and HCI transfer curves were simulated independently using 2D TCAD models shown in Fig. 5. The N region length L_N in ECI model is extended to eliminate the impact of PNP bipolar action. In the same way, HCI model has the P region length L_P extended and the MOS gate removed.

3. Results and Discussion

In order to obtain desired threshold voltages in the proposed model, it is needed to know how design parameters affect ECI and HCI transfer characteristics. In this study, the impact of P region length L_P , P region acceptor concentration N_P , and anode voltage V_A on the proposed model and MGT is examined by TCAD simulations.

Fig. 6(a) shows L_P dependence of ECI transfer curves. Extending L_P decreases the inherent NPN transistor gain and shifts ECI transfer curve upward in high V_P (> 0.5 V) so that when V_G is decreasing, ECI curve in high V_P detaches from HCI curve at higher V_G . As a result, V_{off} of the circuit model rises and the hysteresis width decreases by extending L_P as shown in Fig. 6(b). Fig. 7 shows simulated V_{P} - V_G characteristics of MGT corresponding to the circuit model in Fig. 6. MGT also shows tendency that V_{off} rises and the hysteresis width decreases as L_P is extended. While the circuit model predicts that the hysteresis width is decreased from 0.55 V to 0.40 V by changing L_P from 0.5 µm to 2.0 µm, the actual hysteresis width in MGT is decreased from 0.52 V to 0.34 V.

Fig. 8 shows N_P dependence of ECI transfer curves. Decreasing N_P not only enhances the inherent NPN transistor gain but also lowers the threshold voltage of the inherent MOSFET so that ECI transfer curve starts being modulated at lower V_G (Fig. 8(a)). Consequently, both V_{on} and V_{off} of the circuit model are lowered by decreasing N_P (Fig. 8(b)). Fig. 9 shows V_P-V_G characteristics of MGT corresponding to the circuit model in Fig. 8. It is confirmed that V_{on} and V_{off} of MGT are also lowered by decreasing N_P . By decreasing N_P from 2×10^{18} cm⁻³ to 7×10^{17} cm⁻³, V_{on} is lowered from 1.11 V to 0.38 V, and V_{off} from 0.77 V to 0.19 V. Thus, MGT with low threshold voltages and small hysteresis is achieved by tuning ECI parameters. When V_A is reduced, ECI and HCI transfer curves shift

When V_A is reduced, ECI and HCI transfer curves shift keeping their shapes (Fig. 10(a)) so that V_{on} and V_{off} of the circuit model hardly change (Fig. 10(b)). In the same way, MGT keeps its threshold voltages as V_A varies (Fig. 11(a)). The benefit of V_A reduction for MGT is that on-current is reduced exponentially to V_A (Fig. 11(b)). This means that in PNBTFET, the body terminal voltage and the body current can be suppressed at once, and therefore, the constant power consumption can be greatly reduced. In this simulation, the power consumption is reduced to about 10⁻⁷ times by lowering V_A from 1.0 V to 0.5 V.

When MGT in Fig. 11 turns on, V_P rises by 0.53 V at $V_A = 0.7$ V and by 0.26 V at $V_A = 0.5$ V. When this MGT merges with an SOI MOSFET with $N_P = 7 \times 10^{17}$ cm⁻³ and $T_{OX} = 10$ nm so that it possesses SS of 110 mV/decade, it is estimated that rise in V_P will lower the threshold voltage of the SOI MOSFET by 0.44 V at $V_A = 0.7$ V and by 0.22 V at $V_A = 0.5$ V, and will cause abrupt SS (~ 0 mV/decade) over 4 decades at $V_A = 0.7$ V and 2 decades at $V_A = 0.5$ V. Moreover, it is estimated that the on-state body current will be 5.0 nA at $V_A = 0.7$ V and 2.7 pA at $V_A = 0.5$ V on the assumption that PN body tie width is 1.0 µm.

4. Conclusions

It was confirmed that the voltage-based equivalent circuit model of MGT shows good correlation with MGT characteristics and their response to design parameters L_P , N_P , and V_A . This model will help properly designing steep SS PNBTFETs with low power consumption, by providing insight into the MGT operation mechanism.

References

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Fig. 1 Bird-eye view of PN-Body Tied SOI FET (PNBTFET).









Fig. 4 Schematic transfer curves of HCI and ECI. Stable points indicated by circles may move, appear, or disappear when ECI curve is modulated by V_G .





1.0





V_G characteristics of MGT corre-

sponding to the model in Fig. 6.

Fig. 3 Voltage-based equivalent circuit model of MGT [5].

2.0 µm.

Fig. 6 Impact of L_P variation on (a) transfer curves of ECI and (b) V_P - V_G characteristics decided by ECI and HCI transfer curves. $V_A = 1.0$ V, $N_P =$ 2×1018 cm-3.



(a)



Fig. 8 Impact of N_P variation on (a) transfer curves of ECI and (b) V_P - V_G characteristics decided by ECI and HCI transfer curves. $V_A = 1.0$ V, $L_P =$



Fig. 10 Impact of V_A variation on (a) ECI and HCI transfer curves, and (b) V_P - V_G characteristics decided by ECI and HCI transfer curves. N_P = 7×10^{17} cm⁻³, $L_P = 2.0$ µm.





Fig. 11 Impact of V_A variation on (a) V_P - V_G characteristics and (b) I_A - V_G characteristics of MGT. $N_P = 7 \times 10^{17} \text{ cm}^{-3}$, $L_P = 2.0 \text{ }\mu\text{m}$.