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Achieving BEOL footprint-efficient and low cost monolithic 3D$^+$ IoT chip using low thermal budget laser technology

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Abstract

We have demonstrated a backend of line (BEOL) compatible 3D$^+$ IoT chip that monolithically integrate multi-functional logic and analog units, memories, sensors, energy harvester, and wireless-communication VCO (voltage- controlled oscillator). The sequentially stacked a-SiGeC TFPV device as an embedded ambient light energy harvester can provide electricity to the IoT circuits. The key to realize such miniaturized, self-powered, low cost, multi-functional 3D$^+$ IoT chip is to keep substrate temperature (T_{sub}) lower than 400 ^{o}C using all low temperature and thermal budget laser processes.

1. Introduction:

Heterogeneous 3D integration that can connect multi-functional devices and circuits within a single chip is a promising technology for IoT application. However, conventional through silicon via (TSV) based 3D integration that relies on TSV or bump is more complex and costly. Monolithic 3D (M3D) integration seems a better solution for its higher connectivity, smaller form factor, and potential cost reduction. One example is the monolithic 3D NAND flash by stacking 64 layers of cell arrays [1]. For monolithic logic unit, we can be broadly classified into two groups: a) active layer transfer technology (e.g., CEA-Leti [2], IBM [3], Stanford niversity [4]) and b) direct active layer formation on a single wafer (e.g., AIST [5], UMC [6]).

We have demonstrated a monolithic 3D$^+$IC using various low temperature and thermal budget laser processes (T_{sub}≤400^{o}C) [7][8]. With these processes and integrated circuit design, we can sequentially integrate multifunctional devices, including logic and analog units, sensors, an energy harvester, a wireless-communication VCO (voltage-controlled oscillator), and a RRAM memory array. It paves the way for footprint efficient and low cost IoT chip fabrication.

2. 3D$^+$ device/circuit fabrication and 3D$^+$ IoT chip:

Our BEOL compatible monolithic 3D$^+$IC with 3D stackable single-grained Si FET and multi-layered (M3-M3') tungsten (W) interconnects is illustrated in **Fig. 1.** We introduce three low thermal budget laser process to keep substrate temperature lower than 400^{o}C for BEOL process integration. First, the green nanosecond laser (λ=532nm) helps to prepare large grain and highly crystallized poly-Si film. The following CMP and multi-step modification processes reduce surface roughness and enhance crystallinity of the channel (**Fig. 2**). Second, the far infrared ray laser anneal (FIR-LA, λ=10.6μm) is used to fully activate the high doped and diffusionless source/drain region for scaling devices (**Fig. 3**). Third, two step laser-assisted self-aligned NiSi process with FIR-LA is proceeded for further reducing series and contact resistance of 3D stackable nano-devices (**Fig. 4**).

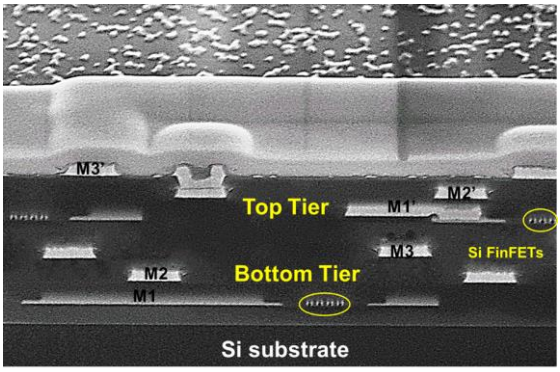

Fig. 1, FIB cross-section of two tiered monolithic 3D$^+$ IC.

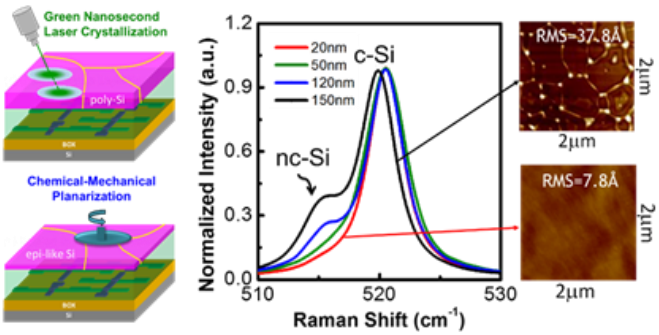

Fig. 2, Illustration of green nano-second laser crystallization and CMP processes for highly crystallized Si channel preparation.

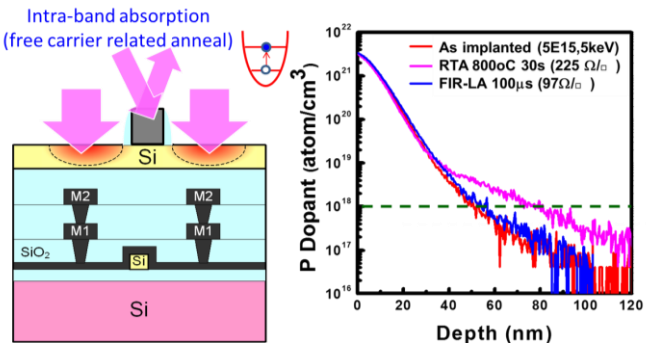

Fig. 3, Far infrared ray laser anneal for highly doped source/drain activation.

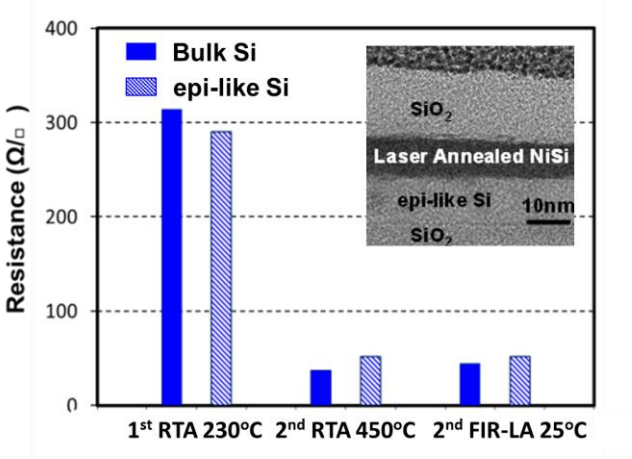

Fig. 4, Far infrared ray laser anneal for Salicide process.

With these low thermal budget laser process, we demonstrated a self-powered fully functionalized monolithic 3D$^+$-IC with light-electricity power management, wireless communication, and high density data-storage modules. The block diagram of the circuit are shown in **Fig. 5**. The a-SiGeC thin film photovoltaic (TFPV) serves as an ambient light energy harvester to generate electricity to the power management unit that converts the 0.5V PV source to three regulated power supplies for the memory, sensor, and radio-frequency (RF) circuits.

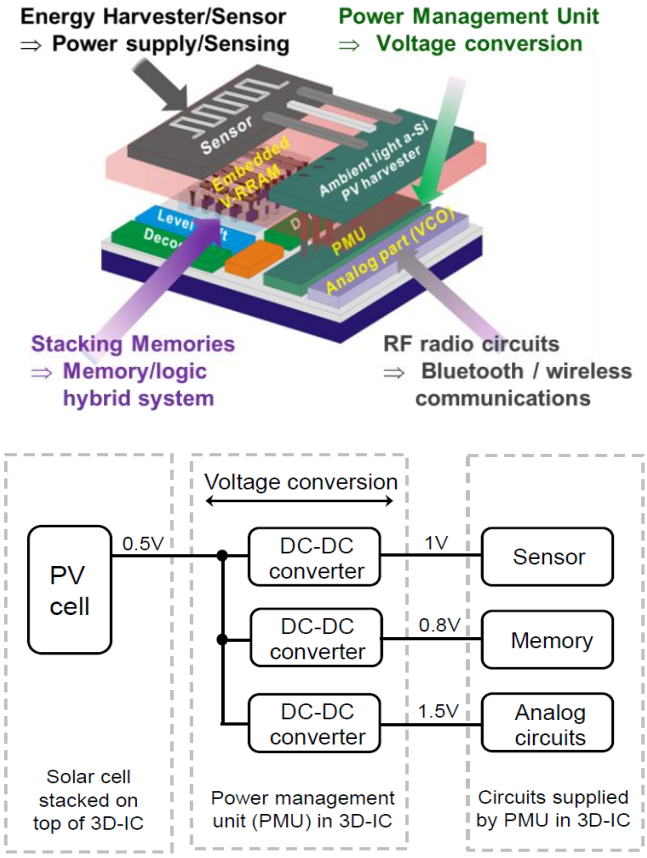

Fig. 5, Illustration and block diagram of the low-cost, low power, high driving current monolithic 3D$^+$ IoT chip including embedded non-volatile memory, communication device, and power controller.

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