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Investigation of the Optimum Stacking Number of Stacked Nanowires for Logic Applications

Wei-Cheng Huang and Pin Su
Department of Electronics Engineering & Institute of Electronics, National Chiao Tung University, Taiwan
E-mail: haunlliam.ee04g@nctu.edu.tw

Abstract

Based on 5-nm technology node, the optimum stacking number for vertically stacked nanowire FETs is investigated considering the impacts of various contact resistivity, supply voltage and vertical pitch on logic performance. Our study indicates that low contact resistivity and low supply voltage are beneficial to more layers of stacked nanowire FETs in terms of switching speed and energy efficiency. Besides, the vertical pitch of nanowires is crucial to the optimum stacking number due to the extra parasitic capacitance.

1. Introduction

For sub 10-nm technology node, the nanowire (NW) gate-all-around (GAA) FET is a promising device candidate due to its superior electrostatic integrity [1]. To increase the drive current per footprint, multi-channel devices by stacking several layers of NWs are considered [2]. 2-stack silicon NW FETs with gate length 24nm had been fabricated using an industry-relevant metal gate process [3].

With technology scaling, parasitic resistance becomes a big challenge due to the difficulty in achieving low contact resistivity [4]. Besides, 3D structures usually experience substantial parasitic capacitance from gate to S/D epitaxy regions. Even though the drive current can be boosted by stacking NWs, how might the circuit performance change with the stacking number has rarely been known and merits investigation. In this work, parasitic RC is considered simultaneously to find the optimum number of stacked NWs regarding switching speed and energy efficiency.

2. Technology Assumption and Methodology

Fig. 1(a) and (b) show the structure of a 3-stack NW FET and there are three NWs in a single layer. In this work, 1-stack to 6-stack NW devices are considered, and we assume that they possess similar structure parameters under a given technology node. The doping concentration in the S/D regions is 3e20/cm^3. The 20-nm vertical pitch of NWs is based on [3]. Gate work-function is adjusted to make the leakage current per NW equal to 1nA. The mobility data is based on [5]. Based on N5 [6], other key structure parameters of NW FETs are listed in Table I. To evaluate the logic performance of the stacked NW FETs, we employ TCAD mixed-mode [7] to simulate 3-stage inverter chains with symmetric CMOS as shown in Fig. 1(c), considering a capacitance load of 153 aF/um [8] between the adjacent stages to account the impact of back-end of line (BEOL).

3. Results and Discussion

Transfer characteristics (I_D-V_{GS}) of the simulated devices with 1-stack to 6-stack NWs and 9e-9 Ωcm^2 contact resistivity (Rc) are shown in Fig. 2. The ON-state current (I_{ON}) of the 6-stack NW FET compared with the single stack NW FET is boosted by only ~2X due to the high S/D parasitic resistance. In addition, as shown in Fig. 3, the front-end of line (FEOL) parasitic capacitance also increases linearly with the stacking number of the NW FETs, and the increasing rate is proportional to the vertical pitch because the S/D region rises with more stacking layers of NWs.

From the circuit switching speed point of view, Fig. 4 shows that the optimum stacking numbers of NW FETs are 2-stack, 2-stack and 4-stack , respectively, with contact resistivity of 9e-9Ωcm^2, 5e-9Ωcm^2 and 1e-9 Ωcm^2 (ITRS) [9]. In other words, the benefit of boosting I_{ON} by stacking NWs is not significant especially for devices with high contact resistivity, which makes low contact resistivity devices in favor of higher stacked NWs. Considering energy efficiency, 2-stack NW FETs in low contact resistivity (1e-9 Ωcm^2) become the optimum choice in terms of the energy-delay product as shown in Fig. 6. High parasitic resistance is also an obstacle to get the benefit of energy efficiency by stacking NWs.

The impact of various supply voltages (V_{DD}=0.6V, 0.5V and 0.325V), are also evaluated in this work. Fig. 7 shows the optimum stacking number increases with decreasing V_{DD} due to less impact of S/D resistance. In addition, energy efficiency can be improved by stacking NWs with lower V_{DD} as shown in Fig. 9. Therefore, it is possible that the inverter chains delay and energy consumption can be improved by lowering contact resistivity and an adequate V_{DD} (Fig. 10).

Even if we can achieve the ITRS spec of low contact resistivity (1e-9 Ωcm^2), we should still pay attention to the extra parasitic capacitance due to additional layers. Fig. 11 compares the switching delay of stacked NW FETs with 20-nm and 30-nm vertical separations. It can be seen that smaller vertical pitch makes devices more tolerant to stacking more NWs (e.g. from 3 to 4 stacks) due to less extra parasitic capacitance.

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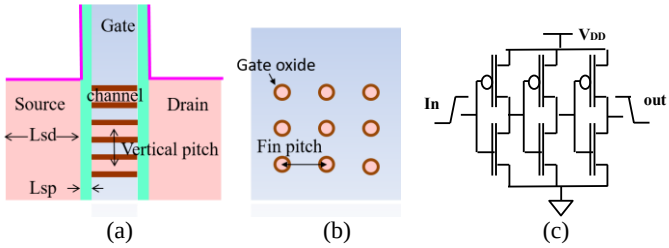

Fig. 1. (a) Schematic of 3-stack NW FET and (b) three NWs in every single layer. (c) The circuit diagram of 3-stage inverter chain.

TABLE I. Structure Parameters [6] used in this work

Gate length (Lg)	10 (nm)	Undoped
Spacer thickness(Lsp)	5 (nm)	K=5
EOT	0.75 (nm)	
S/D extension (Lsd)	12 (nm)	3e20/cm^3
Vertical pitch	20 (nm) [3]	
Fin pitch	16 (nm)	

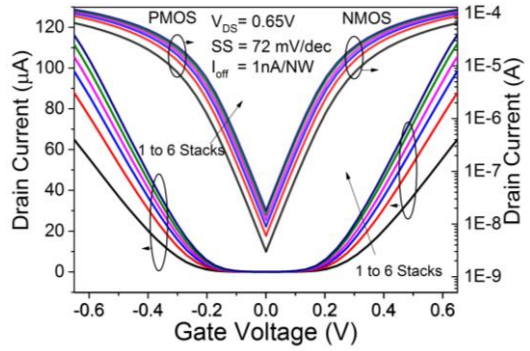

Fig. 2. (a) Transfer characteristics (I_D-V_{GS}) of N-channel and P-channel NW FETs stacked from 1 to 6 layers and each device has equal I_{OFF} per NW.

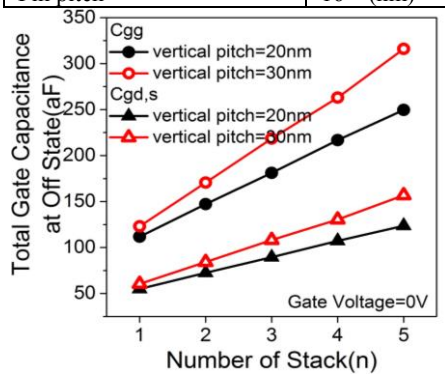

Fig. 3. Total gate capacitance at V_{GS}=0V with various number of stacking considering two vertical pitches, 20-nm and 30-nm.

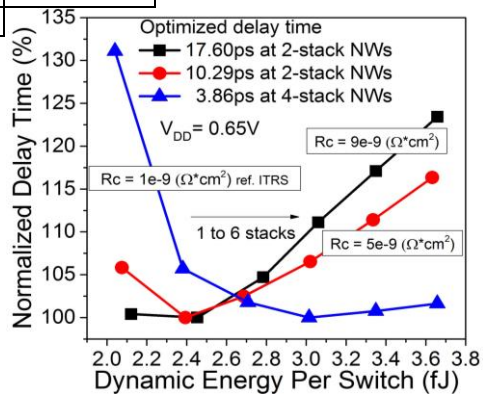

Fig. 4. The inverter chain delay time versus energy consumption per switch with different contact resistivity. The delay times are normalized with the best case shown in the figure.

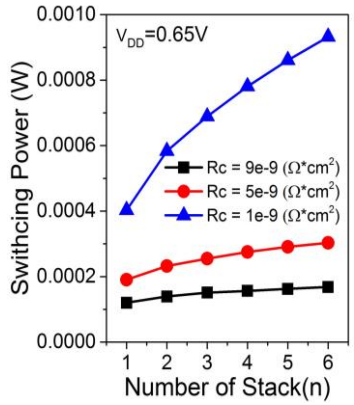

Fig. 5. Comparison of the switching power for NW devices with various stacking number and contact resistivity.

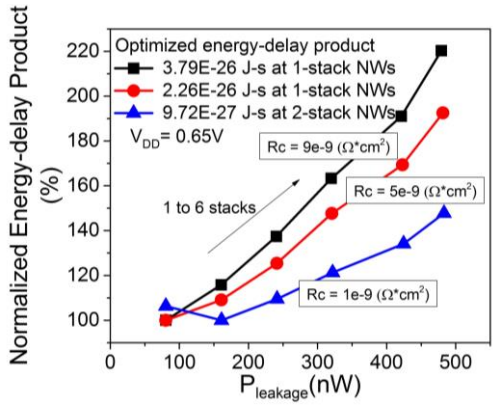

Fig. 6. The inverter chain energy-delay product vs. leakage power. The energy-delay product is normalized with the best case shown in the figure.

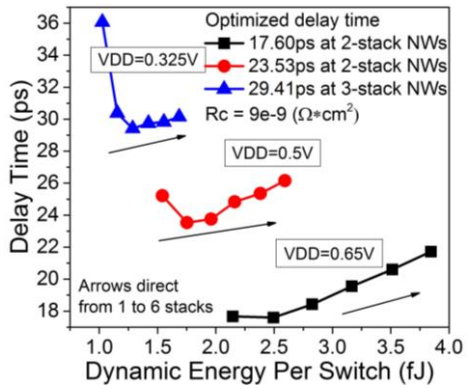

Fig. 7. The inverter chain delay versus energy consumption per switch for V_{DD}=0.65V, 0.5V and 0.325V.

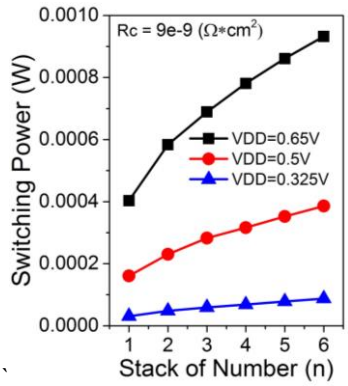

Fig. 8. Comparison of the switching power for NW devices with various stacking number and V_{DD}.

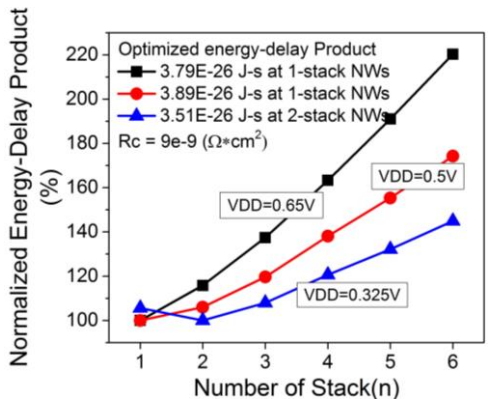

Fig. 9. The inverter chain energy-delay product vs. stacking number for V_{DD}=0.65V, 0.5V and 0.325V. The energy-delay product is normalized with the best case written in the figure

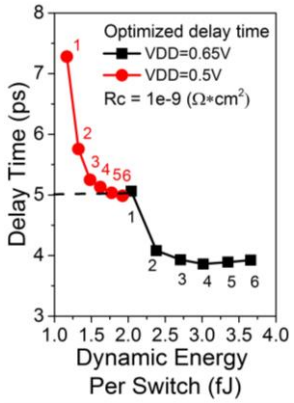

Fig. 10. Delay vs. energy consumption for NW devices with low contact resistivity under V_{DD}=0.65V, and 0.5V.

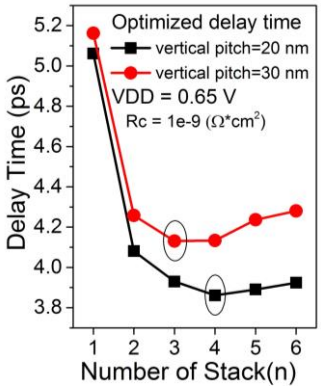

Fig. 11. Comparison of the inverter chain delay for NW devices with vertical pitch=20-nm [3] and 30-nm.