F-1-05

A Compact Sweat Monitoring System with CMOS Capacitive Humidity Sensor for Wearable Health-Care Application

Y. Mitani[1], K. Miyaji[1], S. Kaneko[1], T. Uekura[1], H. Momose[2] and K. Johguchi [1]

[1] Shinshu University, Faculty of Engineering, Department of Electrical and Computer Engineering,
4-17-1 Wakasato Nagano-shi, Nagano, 380-8553, Japan, Phone: +81-26-269-5489 E-mail: johguchi@cs.shinshu-u.jp
[2] Nishizawa Electric Meters Manufacturing Co., Ltd., Sakaki 6249, Sakaki-cho, Hanishina-gun, Nagano, 389-0601, Japan

Abstract

A smart wearable sweat monitoring system is presented with 180-nm CMOS technology. With custom chip and board design, the proposed sweat sensor is integrated into 15 mm×20 mm. From the experimental results, the capacitances of humidity sensor can be accurately measured. As a result, it is verified that the proposed system can used for a human sweat sensor certainly.

1. Introduction

Recently in the medical field, it is attracting attention to monitor human sweat in everyday life in order to estimate neuropathy, heatstroke, dehydration, etc. Although a small resistor-type sweat sensor has been proposed [1], it is difficult to monitor the amount of perspiration. Figure 1 shows a conventional sweat monitoring system [2]. The conventional large and heavy measurement equipment restrains a subject of sweating. Thus, we propose a compact wearable sweat sensor module as shown in Fig. 1. To realize a wearable sensor, it is necessary to designed a costume CMOS chip for capacitive humidity sensor.

2. Capacitive Humidity Sensor Design with CMOS chip

Block Diagram of System and Capacitive Sensor Design

Figure 2 illustrates the proposed wearable sweat sensor system. Two capacitive sensors placed within the air flow path are used to monitor air humidity before/after human skin. Taking a difference between two capacitances (C_{x1} and C_{x2}), which are corresponding relative humidity, absolute humidity can be calculated with eq. (1) [3].

$$H_{\mathrm{abs}} = \frac{348.28 + 93T - 1.36T^2 + 0.086T^3}{13.939\left(T + 273.15\right)} \times H_{\mathrm{rel}} \qquad (1)$$

, where T, H_{abs} and H_{rel} are temperature (°C), absolute and relative humidity, respectively. After calculating H_{abs} difference, amount of sweat can be estimated. Figure 3 depicts a schematic diagram of our proposed circuits. A band-gap reference (BGR) circuit generates a PVT(process-voltage-temperature) tolerant reference current (I_{ref}) and voltage (V_{ref}). A period modulation scheme based on [4] with the supply of I_{ref} and V_{ref} is used to obtain accurate capacitances of C_{x1} and C_{x2}. Here, external capacitors of C_{x1} and C_{x2} are correspond to relative humidity before and after human skin. By measuring four different periods, T_0, T_1, T_2 and T_3, errors due to internal circuits delay and offsets can be eliminated. Note that T_0, T_1, T_2 and T_3 are linked to C_0, (C_{x1}-C_{ref}+C_0), (C_{x2}-C_{ref}+C_0) and (C_{ref}+C_0), respectively.

CMOS Chip and Board Design with Measurement System

Our chip is fabricated with a 180-nm standard CMOS technology as depicted in Fig. 4. A Si-area of prototype is only 0.72 mm^2 including pads. Figure 4 also shows our measurement system with an FPGA board. Although pulse detector for humidity sensor output, $V_{\mathrm{HSENS\text{-}OUT}}$, and period calculator for T_0, T_1, T_2 and T_3 are not integrated into test-chip for reconfigurability, it is realized from synthesis and P&R (place-and-route) results that the FPGA implemented circuits for period measurements is compatible to less than 300 µm×300 µm, which is sufficiently small area for implementation.

3. Experimental Results

Figure 5 gives the measurement results of BGR. From measurements, PVT variations are reduced up to 1.7% for V_{ref} and 1.3% for I_{ref}, respectively. These results secure sufficient accuracy for operating range of the sweat sensor. Figure 6 demonstrates output waveforms monitored by an oscilloscope. From this output waveform, FPGA measures two sets of four periods (T_0 - T_3). After measuring, the FPGA controller pulls up an enable signal of the sensor ($V_{\mathrm{HSENS\_EN}}$) until the next measurement. Figure 7 shows C_{x1} and C_{x2} results obtained from FPGA measurement system. In Fig.7, two capacitance values, C_{x1} and C_{x2}, ought to take the same values because of the same environment although there might be some mismatch. From Fig. 7, the linearity of capacitive sensor is verified. Note that the horizontal axes and insets of Fig. 7 are the humidity and temperature setting values of the chamber. Thus, the real temperature and humidity at sensor devices might be different from settings. Then, Fig. 8 revises the humidity results as absolute value by using eq. (1) and measured temperature value. As shown in Fig. 8, the linarites of C_{x1} and C_{x2} are improved after compensation.

4. Conclusions

A compact sweat sensor system with custom CMOS chip is presented for wearable application. The fabricated chip is, only 0.72 mm^2 with 180 nm CMOS technology. The measurement system has been developed with FPGA and successfully demonstrated capacitive sensor measurements. From the measurement, the proposed system can obtain the certain humidity and be applicable to a human sweat sensor.

Acknowledgements

We would like to express sincere thanks to Nagano pref. technological seeds development program and all the contributors, T. Yoshihara. The VLSI chips in this study have been fabricated in the program of VDEC, the University of Tokyo in collaboration with Rohm Co., LTD., Cadence Design Systems Inc., Synopsys Inc., and Mentor Graphics Co..

References

[1] Q. Gao, *et. al.*, *Nature* **529** (2016) 509. [2] H. Momose, *et. al.*, *IEICE Tech. Report*, **MBE2008-39** (2008) 69, *in Japanese*. [3] M. Sakaguchi, *et al.*, *Proc. JSME ROMOMEC2008* (2008) 1A1-I02 (1)-(2). [4] Z. Tan, *et al.*, *IEEE JSSC* **47**, 7 (2012) 1703.

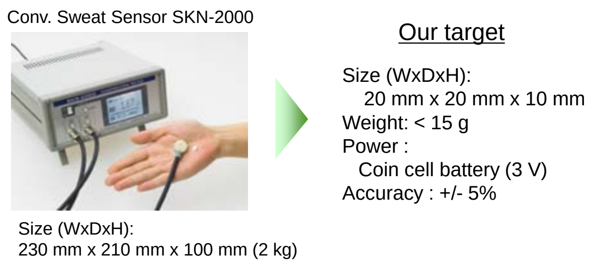

Fig. 1 Conventional sweat sensor product and our target.

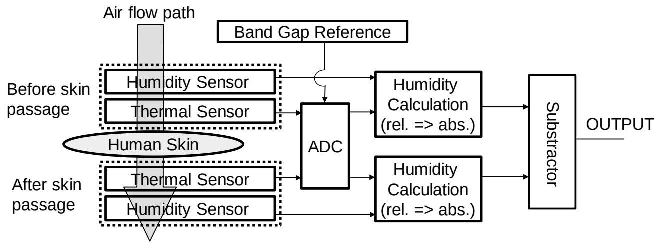

Fig. 2 Block diagram of a wearable sweat sensor.

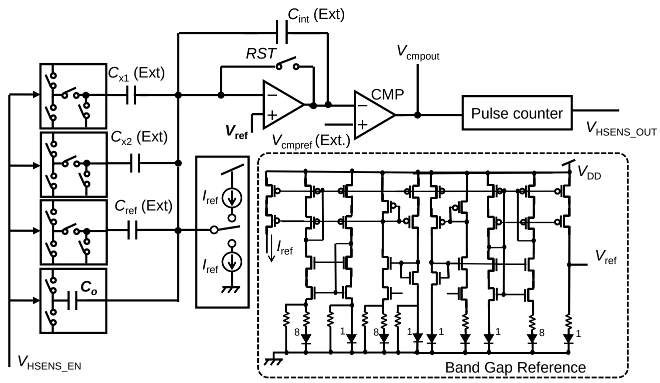

Fig. 3 Schematic diagram of designed circuits.

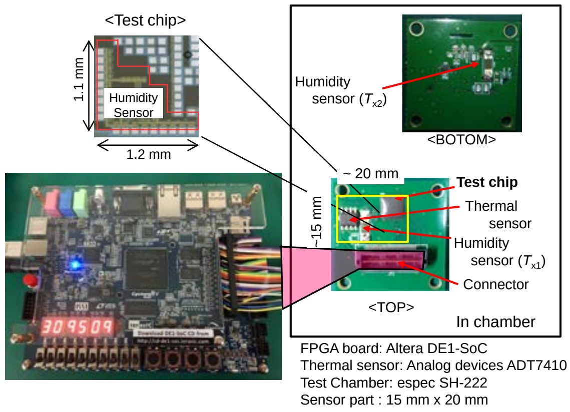

Fig. 4 Measurement setup

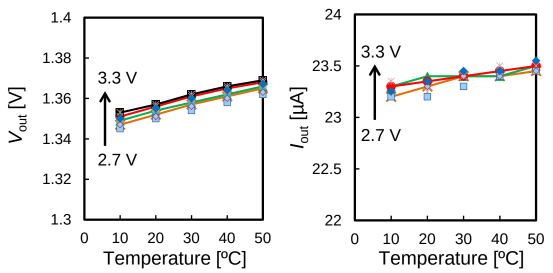

Fig. 5 Measured output (V_{out} & I_{out}) variations of band gap reference circuits.Under voltage and temperature variations, V_{out} and I_{out} variations are suppressed by 1.8% and 1.3%, respectively.

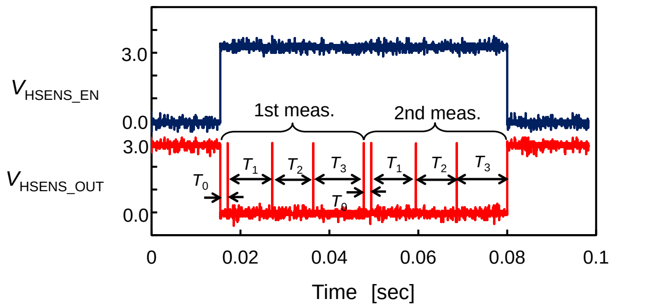

Fig. 6 Waveforms of sensor output (V_{HSENS_OUTPUT}) and control signal (V_{HSENS_EN}) captured by oscilloscope (a) and Logic analyzer output of FPGA (b). The developed FPGA measurement system successfully measured periods of V_{rstint}, which are correspond to C_{x1}, C_{x2} and C_{ref}., which are correspond to C_{x1}, C_{x2} and C_{ref}.

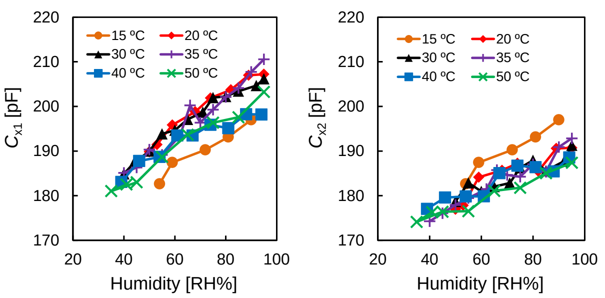

Fig. 7 Measured output (V_{out} & I_{out}) variations of band gap reference circuits.Under voltage and temperature variations, V_{out} and I_{out} variations are suppressed by 1.8% and 1.3%, respectively.

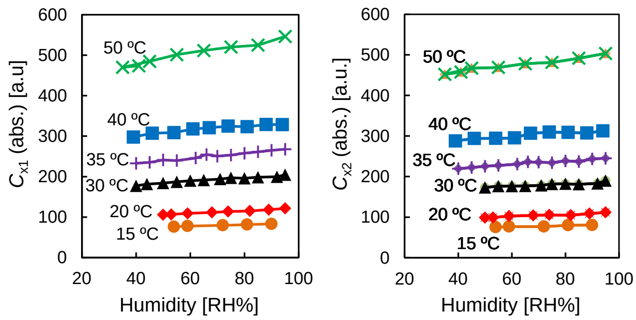

Fig. 8 Measured output (V_{out} & I_{out}) variations of band gap reference circuits.Under voltage and temperature variations, V_{out} and I_{out} variations are suppressed by 1.8% and 1.3%, respectively.