G-5-02

Impact of Drain Current to Appearance Probability and Amplitude of Random Telegraph Noise in Low Noise CMOS Image Sensors

Shinya Ichino[1], Takezo Mawaki[1], Akinobu Teramoto[2], Rihito Kuroda[1], Hyeonwoo Park[1], Takeru Maeda[1], Shunichi Wakashima[1], Tetsuya Goto[2], Tomoyuki Suwa[2] and Shigetoshi Sugawa[1,2]

[1] Graduate School of Engineering, Tohoku University, [2] New Industry Creation Hatchery Center, Tohoku University.
6-6-11, Aza-Aoba, Aramaki, Aoba-ku, Sendai 980-8579, Japan
Phone: +81-22-795-4833 E-mail: shinya.ichino.s1@dc.tohoku.ac.jp

Abstract

In this paper, the impact of drain current to appearance probability and amplitude of random telegraph noise (RTN) in low noise CMOS image sensors (CIS) is clarified using an array test circuit. It is shown that the in-pixel source follower (SF) operation at low drain current is effective for reducing appearance probability of RTN for low noise CIS.

1. Introduction

RTN occurs at in-pixel SF transistors is one of the most critical problem for CIS[1]. Especially, RTN is becoming the limiting factor of low noise performance in high-sensitivity CIS. RTN in MOSFET is caused by capture/emission of the carriers by/from traps in the gate insulator film[2], and it is characterized by the parameters such as amplitude, mean time-to-capture $<\tau_c>$ and mean time-to-emission $<\tau_e>$. The drain current in SF is one of the important parameters for CIS operation regarding the pixel output speed, power consumption and so on. The dependency of drain current to RTN has been reported that the lower current induces larger noise values[3], however the noise floor of the employed measurement system was large. The dependency of drain current to RTN in low noise region has not been fully understood yet. In this study, an impact of drain current ranging from 0.1μA to 11μA to appearance probability and amplitude of RTN is discussed using the developed very low noise measurement system.

2. Experimental Setup

Fig. 1 shows the block diagram of the array test circuit. It was fabricated by a 1P5M 0.18 μm CMOS with pinned photodiode technology. There are in total of $384^{H}\times299^{V}$ cells in this array test circuit with various SF formation conditions. The gate oxide thickness, the gate length and the gate width of the SF transistors of the measured unit cell type are 7.8 nm, 0.52 μm and 0.34 μm, respectively. These are buried channel transistors[4], which is effective for reducing RTN. 18,048 MOSFETs were measured. In the column circuit, there are two readout paths used for different measurement modes. In this measurement, a path directly connected to chip output buffer was used for high-speed signal sampling for selected cells. Fig. 2 shows the low noise measurement system and its performance. In this measurement system, a low floor noise of 35 μV_{RMS} was obtained.

3. Results and Discussions

Fig. 3 shows the cumulative probability of the V_{RMS} in the Gumbel plot. The output voltages were set at 1.9 V for each drain current condition. In the range of cumulative probability about 99.9% and more, the distribution of V_{RMS} is larger for smaller drain current, which agrees to the previous report[3]. On the other hand, in the range of cumulative probability about 90% to 99.9%, the distribution of V_{RMS} is larger for larger drain current, which could not be seen in the previously reported data. Fig. 4 shows the output voltage waveforms extracted at the cumulative probability of 99.99% and 99% in each drain current condition. Comparing (a), (b) and (c), at the cumulative probability of 99.99%, a larger RTN amplitude was observed when drain current becomes smaller. Comparing (d), (e) and (f), at the cumulative probability of 99%, the tendency was opposite and when drain current was 0.1μA, RTN was not observed. Table II shows the number of extracted RTN in 18,048 n-MOSFETs for each drain current condition. It is clear that when drain current becomes larger, the appearance probability of RTN and the proportion of the RTN with multi trap becomes larger. Fig. 5 shows the relative appearance probability histogram of $<\tau_e>$, $<\tau_c>$ and $<\tau_e>/<\tau_c>$ of two states RTN for each drain current condition, respectively. The distributions of relative appearance probability of these time constants and time constant ratio do not change very much among the measured drain current conditions. The obtained result shows that the difference of distribution of V_{RMS} in Fig. 3 is not due to change of time constants. Fig. 6 shows the cumulative probability of the amplitude of two states RTN. When drain current is large, the appearance probability of RTN with small amplitude is large. On the other hand, when the drain current is small, it is observed that a large amplitude of RTN occurs in a very small number of cells, however the appearance probability of RTN decreases under a certain threshold (in this case the detection limit of amplitude). This means, with a given strict criteria of noise, appearance probability of the RTN is smaller for lower drain current. Fig. 7 shows the schematic illustration of the impact of drain current to appearance probability and amplitude of RTN. In order to explain the obtained results, channel percolation model is incorporated. Suppose two transistors each contains a trap that can induce RTN, and the number of percolation paths increases as drain current increases. For Tr.1, the one of percolation paths is influenced by the trap in both drain current conditions. It is considered that the amplitude of RTN becomes large at 0.1μA than 11μA because of the smaller number of percolation path. That is a reason why RTN with large amplitude tends to be observed in small drain current. For Tr.2, it is considered that the trap does not influence the percolation path at 0.1μA, but it does at 11μA, leading to a higher appearance probability of RTN at larger drain current. The higher proportion of multi trap RTN at larger drain current also supports this model. The obtained result shows the SF operation at low drain current condition, for example floating capacitor load readout operation [5], is effective for low noise CIS with small power consumption.

4. Conclusion

In this paper, by evaluating the array test circuit using very low noise measurement system, it was demonstrated that the SF operation at low drain current is effective for reducing appearance probability of RTN in the range of low V_{RMS}. These finding are important for the design and operation of in-pixel SF circuit for low noise CIS.

References

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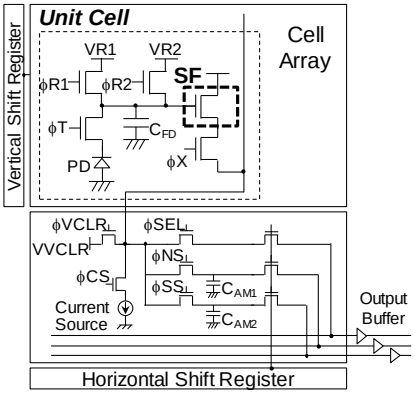

Fig. 1 Block diagram of the array test circuit.

Table I Array test chip design and measured SF specifications.

Array test chip design specifications		Measured SF specifications	
Die size	4800 μm^{H} × 4800 μm^{V}	W/L	0.34 μm / 0.52 μm
Cell size	10 μm^{H} × 10 μm^{V}	Tox	7.8 nm
Number of total cells	384^{H} × 299^{V}	Number of measured cells	384^{H} × 47^{V} (18048)

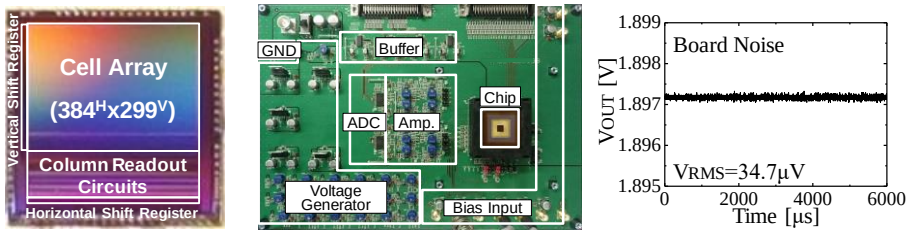

Fig. 2 Low noise measurement system. (a) Picture of the array test chip, (b) picture of the measurement board and (c) the low noise performance of the measurement board.

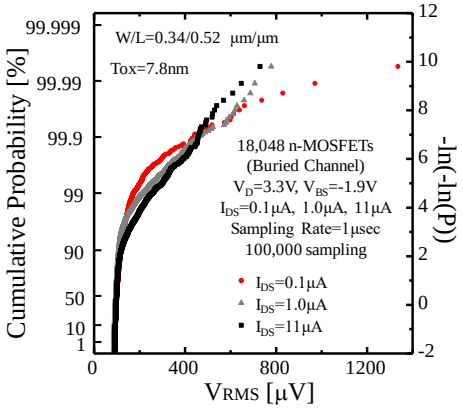

Fig. 3 Cumulative probability of the V_{RMS}.

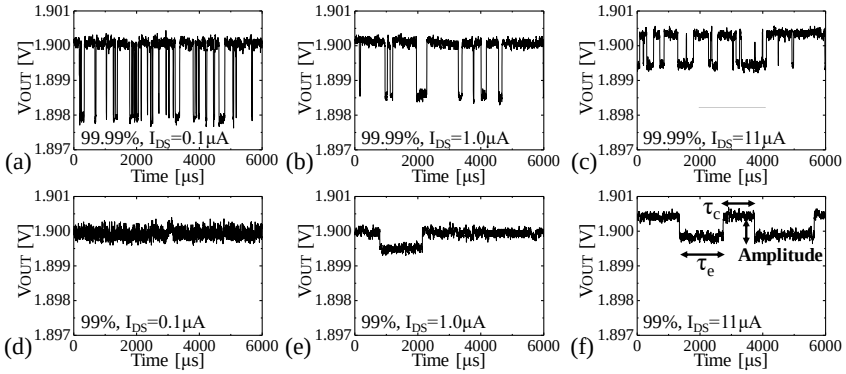

Fig. 4 Output voltage waveforms extracted at the cumulative probability of (a)~(c) 99.99% and (d)~(f) 99% in each drain current condition.

Table II The number of extracted RTN in 18,048 n-MOSFETs for each drain current condition.

	0.1 μA	1.0 μA	11 μA
2 states	366 (99.2%)	612 (99.3%)	1113 (98.0%)
3 states	2 (0.5%)	3 (0.5%)	16 (1.4%)
More than 4 states	1 (0.3%)	1 (0.2%)	7 (0.6%)
Total	369	616	1136

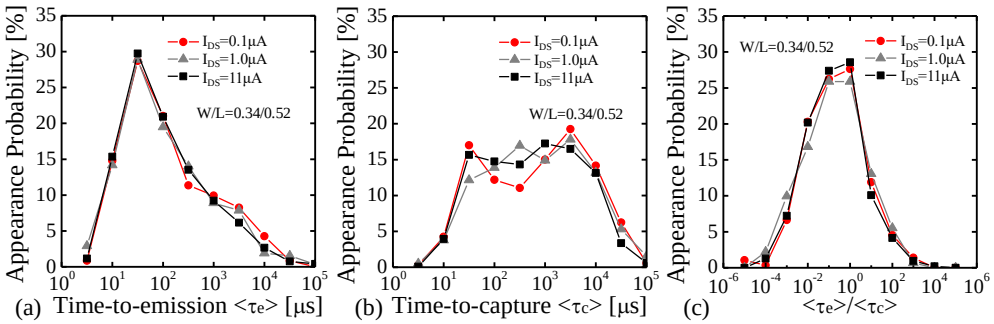

Fig. 5 (a) Relative appearance probability histogram of (a) mean time-to-emission <τe>, (b) mean time-to-capture <τc> and (c) <τe>/<τc> of two states RTN for each drain current condition.

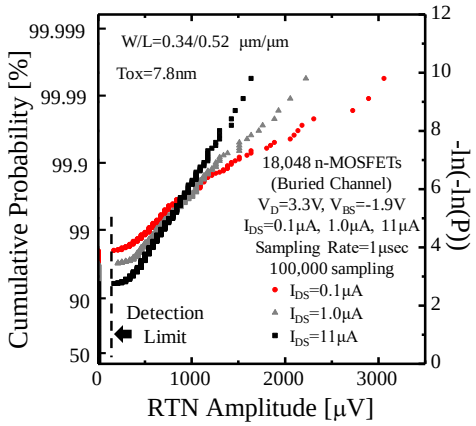

Fig. 6 Cumulative probability of the amplitude of two states RTN.

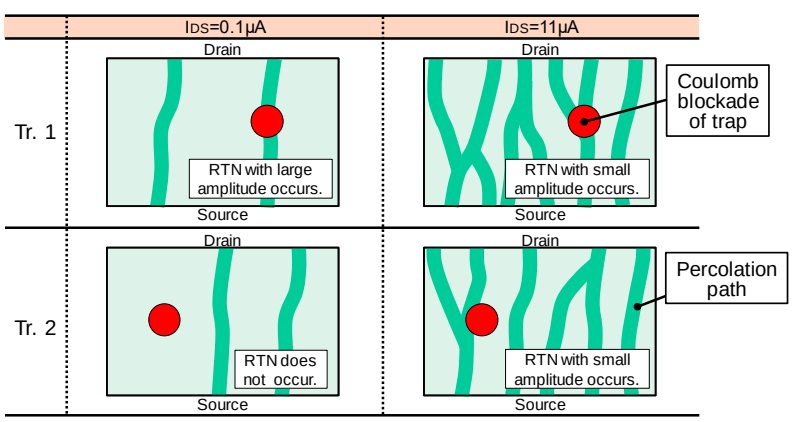

Fig. 7 Schematic illustration of the impact of drain current to appearance probability and amplitude of RTN.