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Analysis of Random Telegraph Noise Behaviors of nMOS and pMOS toward Back Bias Voltage Changing

Takezo Mawaki[1], Akinobu Teramoto[2], Rihito Kuroda[1], Shinya Ichino[1], and Shigetoshi Sugawa[1, 2]
[1] Graduate School of Engineering, Tohoku Univ., [2] New Industry Creation Hatchery Center, Tohoku Univ.
6-6-10 Aza-Aoba, Aramaki Aobaku, Sendai, 980-8579, Japan
Phone: +81-22-795-4833 E-mail: takezo.mawaki.r2@dc.tohoku.ac.jp

Abstract

This paper presents experimental analysis of random telegraph noise (RTN) behaviors toward back bias voltage changing for nMOS and pMOS fabricated by a 0.22μm CMOS technology. It was clarified that statistically the noise distribution is smaller for pMOS than nMOS for all the back bias conditions. However, the dependency of RTN amplitude and time constant on back bias voltage is highly different for each transistor.

1. Introduction

Random telegraph noise (RTN) is one of the origins of low frequency noise in MOSFETs. RTN has become a major issue in scaled down technologies. The phenomenon is characterized by a discrete and random fluctuation of conductance in carrier transport and the number of conduction carriers, caused by the capture/emission of the conduction carrier by/from individual traps in an insulator film or bulk material[1]. The RTN amplitude and time constants are important parameters to identify traps which cause RTN[2-3]. From previous studies, it was revealed the dependence of amplitude and time constants on the gate-source voltage (V_{GS}) can be determined by the number of carriers, distance between the trap and percolation path and the trap energy level[3-4]. In analog circuits, effects of back bias (V_{BS}) is especially important. Thus, the characteristics of RTN toward various V_{BS} should be studied in detail for the design of low noise analog circuits. However, little has been reported on RTN dependence on V_{BS} so far[5]. In this study, using the developed high speed, high precision noise measurement system with array test circuit, behaviors of RTN toward V_{BS} changing are analyzed for both nMOS and pMOS from a large number of samples.

2. Experimental

Fig. 1 shows the schematic of the array test circuit[5], fabricated by a 0.22μm 1P2M CMOS technology. Using the test circuit, measurement is carried out by reading the output voltage (V_{out}), under a constant drain current. RTN appears as the voltage fluctuation of the V_{out} which is the source terminal voltage of the measured MOSFET. Fig.2 shows the measurement sequence in this work. The measurement number is 2048 for both nMOS and pMOS. To detect MOSFETs with RTN, a root mean square of V_{out} in time domain (V_{RMS}) was extracted with the sampling period of 2.5μsec. For the detailed analysis toward V_{BS}, first the MOSFETs of which V_{RMS} were greater than 1mV with two states RTN were extracted. For the extracted 20 nMOS and pMOS, I_D-V_{GS} curves were obtained by sweeping V_{BS} and I_D. By using the obtained I_D-V_{GS} curves, $|V_{GS}|$ was set constant at 0.6V for different V_{BS} conditions for each MOSFET. The V_{BS} was varied for over 1V for both nMOS and pMOS. The RTN parameters: the time stays at high $|V_{GS}|$ state (τ_H), the time stays at low $|V_{GS}|$ state (τ_L) and the amplitude were extracted accurately with sampling period of 2.5μsec and record time of 5sec. Average values of τ_H and τ_L were extracted by fitting the distribution of extracted τ_H and τ_L assuming these phenomena follow the Poisson process [1].

3. Results and Discussions

Figs. 3 and 4 show (a-b) the RTN amplitude as a function of V_{BS} and I_D, and (c-d) $<\tau_H>$ and $<\tau_L>$ as a function of V_{BS} for the measured nMOS and pMOS, respectively. Here I_D changes by changing V_{BS} under a constant V_{GS} due to the body effect and mobility change. The dependencies of amplitude are quite different among transistors for both nMOS and pMOS cases. For example, the RTN amplitudes in some of the transistors increases as $|V_{BS}|$ increases, and the others decreases. The tendencies are somewhat different between nMOS and pMOS. That is, for majority of the measured pMOS the amplitude becomes smaller for higher $|V_{BS}|$ even though the drain current is smaller. For nMOS, the portion of transistors are about the same with tendencies of increasing and decreasing amplitude for increasing $|V_{BS}|$. Regarding the time constants, for almost all cases, $<\tau_L>$ increase as the increase of $|V_{BS}|$ and decrease of I_D. The obtained tendency is reasonable supposing $<\tau_L>$ depends on the potential barrier from the channel to the trap and number of channel carriers. On the contrary, for $<\tau_H>$, more diverse characteristics were obtained toward $|V_{BS}|$ change. Fig.5(a-b) show correlation plots between RTN amplitudes in two $|V_{BS}|$ for nMOS and pMOS, respectively. RTN amplitude tends to become smammer for larger $|V_{BS}|$ in both nMOS and pMOS cases. It should be noted that plots at 0 means RTN disappeared at the corresponding $|V_{BS}|$. Fig.6 shows the cumulative probability of V_{RMS} in Gumbel plot for two $|V_{BS}|$ for nMOS and pMOS. The noise distribution of pMOS is smaller than nMOS at each $|V_{BS}|$ condition. For both nMOS and pMOS, a larger $|V_{BS}|$ results in an increase of noise distribution. The higher $|V_{BS}|$ and lower I_D results in narrowing of channel in depth direction and smaller number of channel carriers, these factors are considered to increase the impact of traps overall.

In order to explain the behaviors of RTN amplitude toward $|V_{BS}|$, schematic illustrations of percolation path and its behavior toward $|V_{BS}|$ changing are shown in Fig.7. The number of randomly distributed ionized acceptors in depletion layer increases as $|V_{BS}|$ increases. Due to this, sometimes a portion of channel carriers in a percolation path close to traps which cause RTN decreases or percolation path itself may disappear, which lead to a decrease of RTN amplitude.

4. Conclusions

Behaviors of RTN in toward back bias changing were analyzed for nMOS and pMOS in this work. Statistically, pMOS has smaller noise distribution than nMOS at each back bias, and larger back bias results in an increase of noise distribution for both nMOS and pMOS. However, the dependency of RTN parameters such as amplitude differ among transistors. A further study of understanding the effect of channel percolation change due to the applied back bias is needed.

References

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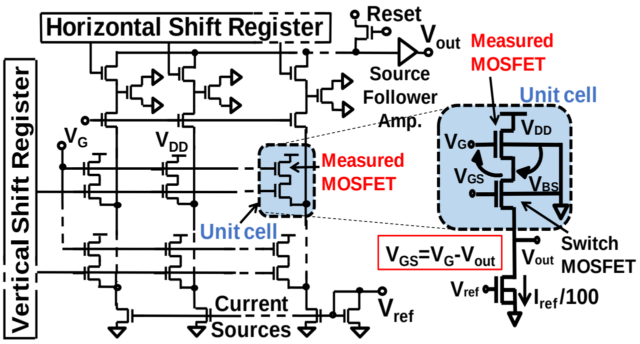

Figure 1. Arrayed test circuit diagram.

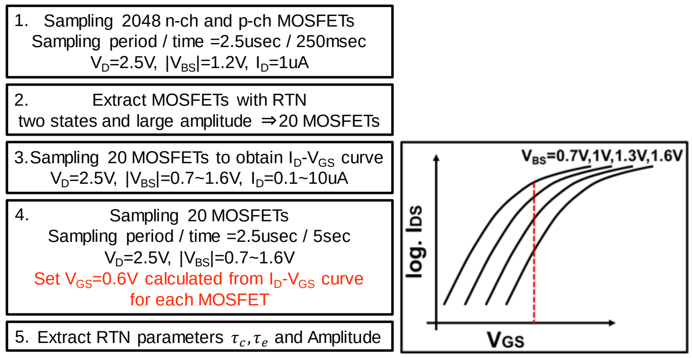

Figure 2. Measurement sequence and I_D-V_{GS} curve

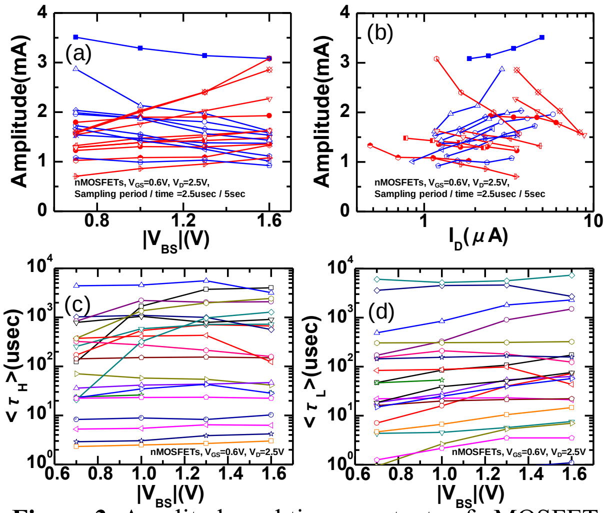

Figure 3. Amplitude and time constants of nMOSFET as a function of V_{BS} and I_D. (a) Slopes of Amplitude vs. V_{BS}, (b) Slopes of Amplitude vs. I_D, (c) Slopes of τ_H vs. V_{BS} and (d) Slopes of τ_L vs. V_{BS}.

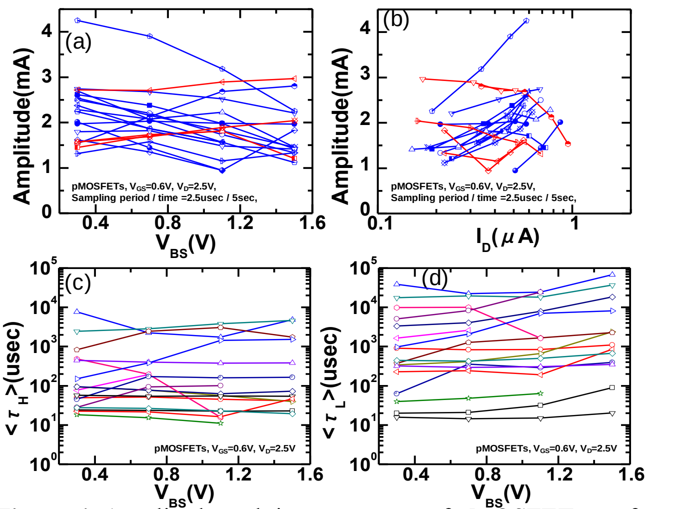

Figure 4. Amplitude and time constants of pMOSFET as a function of V_{BS} and I_D. (a) Slopes of Amplitude vs. V_{BS}, (b) Slopes of Amplitude vs. I_D, (c) Slopes of τ_H vs. V_{BS} and (d) Slopes of τ_L vs. V_{BS}.

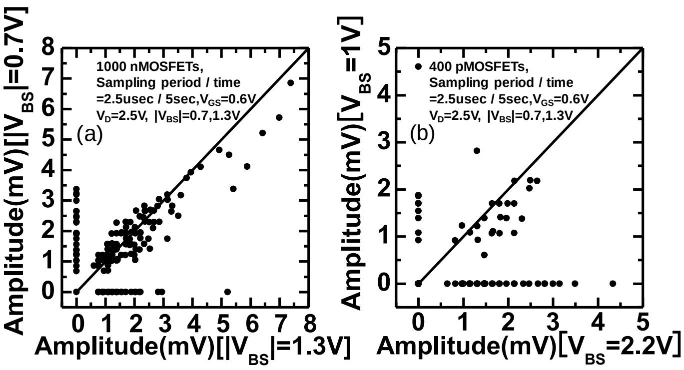

Figure 5. Correlation diagram of large and small V_{BS}. (a) nMOSFETs, (b) pMOSFETs.

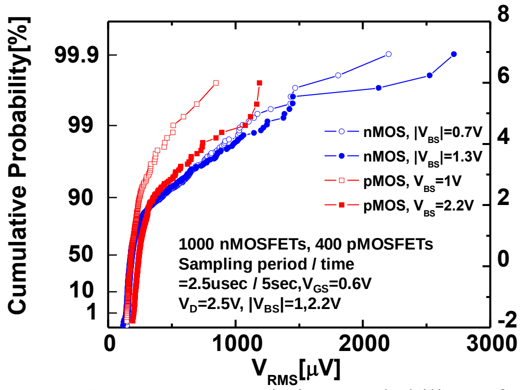

Figure 6. Cumulative probability of V_{RMS} in Gumbel plot for two V_{BS}.

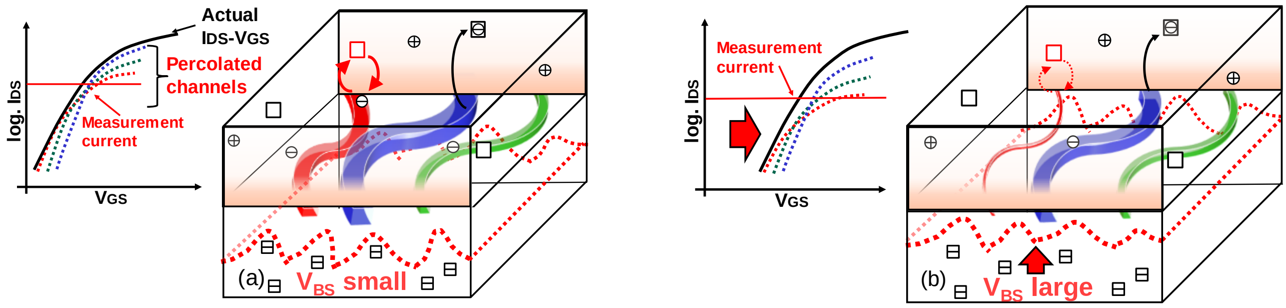

Figure 7. Schematic illustration of the percolated channel and its effect to the I_D-V_{GS} characteristics and RTN. (a) shows the condition of small V_{BS}. (b) shows the condition of large V_{BS}.