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Fully Digital Ternary Content Addressable Memory using Ratio-less SRAM Cells and Hierarchical-AND Matching Comparator for Ultra-low-voltage Operation

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Abstract

A 36-bit x 32-entry fully digital ternaly content addressable memory (TCAM) using the Ratio-less 12-transistor SRAM (RL-12T-SRAM) technology and fully complementary hierarchical-AND matching comparators (HAMCs) was developed for ultra-low-voltage operation. The minimum operating supply voltage of 0.25V which is the less than half of the conventional TCAM was experimentally confirmed by the developed test chip.

1. Introduction

The content addressable memory (CAM) is a specialized memory that searches for the specified data and answers the address if the data is stored. Especially the ternary CAM (TCAM) can store the three values of '0','1' and 'X' (Don't care) and performs the longest prefix matching with the wildcard masks [1]. Since the TCAM features super high-speed searching by the parallel hardware processing, it is mainly used in the network routers for classifying the fast packets. TCAMs are expected to be applied to the big-data-processing, however, its huge power consumption is a serious constraint.

2. Ratio-less TCAM Cell Design

We had developed the Ratio-less 12-transistor SRAM (RL-12T- SRAM), as shown in Fig.1, in which the design margin, such as Static Noise Margins is no longer considered [2]. Its full-complementary and digital operation enables to avoid the influence of device variabilities, therefore it can operate with a quite low supply voltage. Figure 2 shows a conventional TCAM cell with two 6T-SRAM cells in which the data comparator drives the common match line dynamically and the match line sense amplifier (MLSA) detects the entry is match or not [3].

Figure 3 shows the developed ratio-less TCAM (RL-TCAM) cell. In a TCAM cell, high-speed read operation and the handling of the half-select state as in SRAM are unnecessary, therefore the read bit-line (RB) driver in the RL-12T-SRAM cell can be eliminated (see Fig.1). As a result, the number of transistors for 1-bit storage is reduced from 12 to 8. The comparison of TCAM cells is summarized in Table. 1. In the SRAM cell, twice the number of transistors is required to construct a ratio-less cell, on the other hand, in the RL-TCAM cell the number of transistors is reduced from 32 to 24. In addition, the layout area becomes less than 1.5 times of the conventional TCAM cell. This is because the ratio-less design allows to employ minimum dimension for each transistor.

3. Structure of TCAM

Since the dynamic operation of the MLSA scheme in conventional TCAM is suffered from the device variabilities especially in the low supply voltage range, we have developed a full complementary hierarchical AND matching comparator (HAMC) for the RL-TCAM. The block diagram of the RL-TCAM is shown in Fig. 4. The TCAM array is configured with 36-bit x 32-entries. The HAMC is embedded into the TCAM array. Figure 5 shows the comparison of power consumption versus supply voltage between the conventional TCAM with MLSA scheme and RL-TCAM with HAMC using the Monte Carlo analysis. In conventional scheme, all of the match lines are pre-charged and almost of the matched lines are dis-charged in every cycle. On the other hand, in the RL-TCAM, static logic enables the low voltage operation and prevents the waste of power. Figure 6 shows the optimized Wp/Wn ratio and the delay time for CMOS logic gates for Vdd = 1.8V and for Vdd = 0.25V, respectively. Because the delay time of NOR gates too large to use in low voltage region, HAMC consists of the series connection of the AND (NAND and INVERTER) gates.

4. Chip development and experimental results

A test chip incorporating a conventional TCAM with 6T-SRAM cells and MLSA, and a proposed RL-TCAM with RL-TCAM cells and HAMC was developed using a 0.18um CMOS as shown in Fig.7. Figure 8 shows the measured results of TCAMs that are tested with the randomly generated data and search keys. Although the operating speed is almost same in the Vdd > 0.6V, however the minimum operating voltage of RL-TCAM reaches 0.25V, which is less than the half of the conventional TCAM of 0.60V. These measured results are agree with the measured results of SRAMs evaluated in the Ref.2.

5. Conclusions

RL-TCAM using 24-transistor ratio-less TCAM cells with and fully complementary HAMC was developed for ultra-low-supply voltage operation. The minimum operating voltage of 0.25V of developed RL-TCAM which is less than half of conventional TCAM was confirmed by measurements of the test chip.

Acknowledgment

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References

[1] K. Pagiamtzis, A. Sheikholeslami, “Content Addressable Memory (CAM) Circuits and Architecture: A Tutorial and Survey”, IEEE Journal of Solid-State Circuits, Vol.41, No.3, March 2006

[2] T. Kondo et.al., “Ratio-less full-complementary 12T SRAM for Ultra Low Supply Voltage Operation”, Japanese Journal of Applied Physics 54, 04DD11, March 2015

[3] Nitin Mohan et.al.," A Low-Power Ternary CAM With Positive-Feedback Match-Line Sense Amplifiers", IEEE Transactions on Circuits and Systems I, Vol.56, pp.566-573, April 2009.

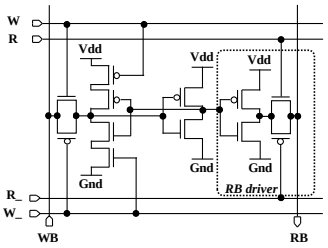


Fig.1 Ratio-less 12-transistor SRAM cell [2]

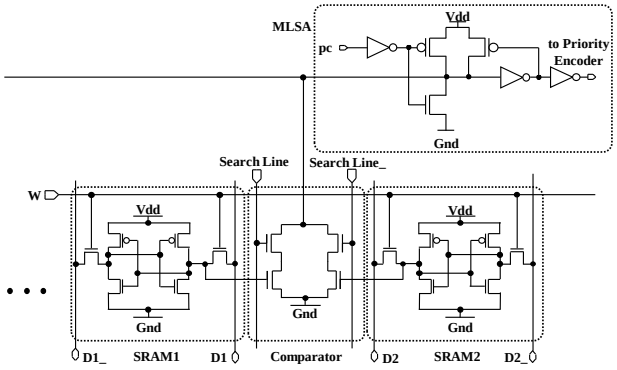


Fig.2 Conventional TCAM cell

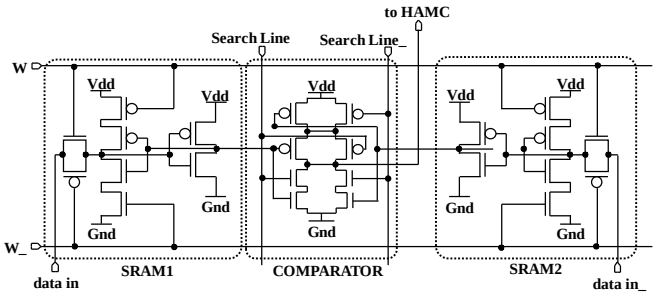


Fig.3 Ratio-less TCAM cell

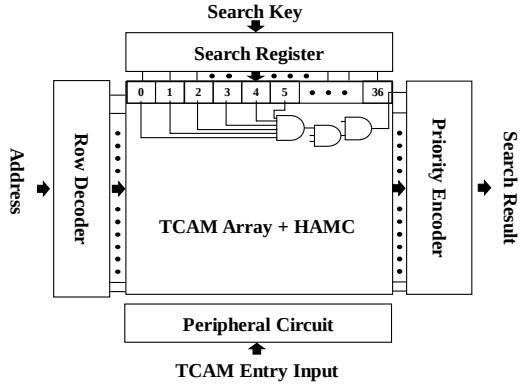


Fig. 4 Block diagram of RL-TCAM

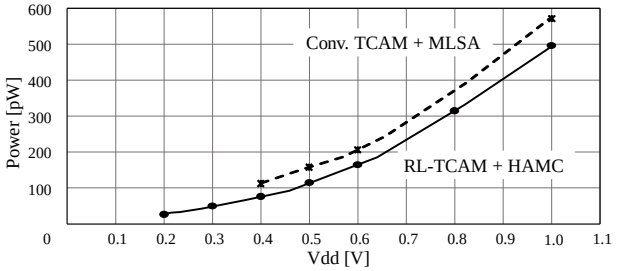
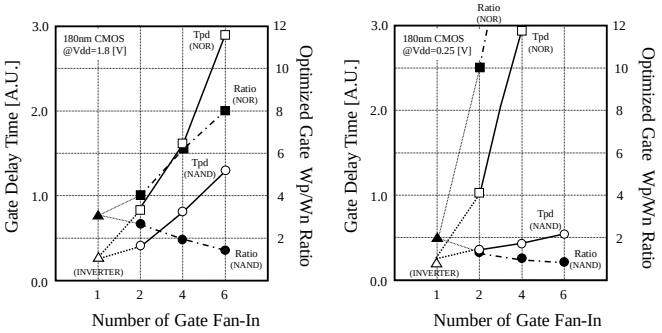
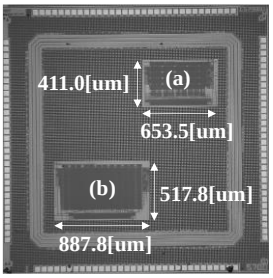


Fig.5 Comparison of the power in the matching operation



(a) Vdd = 1.8 [V] (b) Vdd = 0.25 [V]

Fig.6 Optimized Wp/Wn Ratio and Delay Time for CMOS Gates



(a) Conventional TCAM (b) RL-TCAM

Fig.7 Photo of developed test chip

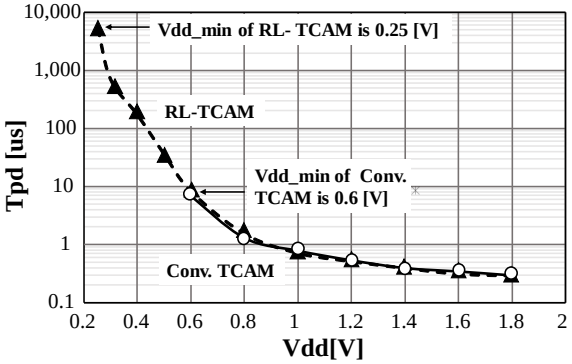


Fig.8 Measured minimum operating voltage

Table. 1 Summary of the comparison between conventional TCAM and RL-TCAM

	Conventional Design	Ratio-less Design	overhead
SRAM cell[2]	6 [TRs]	12 [TRs]	x 2
TCAM cell	16 [TRs]	24 [TRs]	x 1.5
TCAM cell (Area)	70.4 [um^2]	102 [um^2]	x 1.45