Extended Abstracts of the 2017 International Conference on Solid State Devices and Materials, Sendai, 2017, pp343-344

High Volume Testing and Calibration Technique of CMOS Analog Circuits for System-on-Chips and Microprocessors

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Abstract

This paper presents the high volume testing and the calibration technique for the on-die CMOS analog components of the system-on-chips (SOCs). The DC voltage measurement circuit, together with the DC offset voltage trimming circuit was developed as a generic design-for-test (DFT) solution of the on-die analog components. The proposed method can achieve the DC offset voltage trimming with better accuracy and the robustness than the traditional approaches, and it is suitable for high volume manufacturing (HVM). The performance of the feature was verified by the measurement of 10731 silicon units that were manufactured on 14nm CMOS.

1. Introduction

Modern system-on-chips (SOCs) tend to integrate many of the on-die digital and analog intellectual properties (IPs) on a single chip die. In spite of the fact that the high volume testing method of the on-die digital IPs is fully established, it's still quite a challenge on the high volume testing and the calibration of the on-die analog IPs, for the test time, the test coverage, the accuracy, and the robustness. As a traditional analog DFT method, a couple of package pins were allocated for the direct voltage measurement of the internal analog circuits, but this method shows a difficulty in recent generations, because the number of the analog components on a single chip die increases in each generation, while the number of the package pins is limited. The authors developed a very compact ADC to resolve this issue [1]. This ADC has a very compact silicon area of only 500 square microns on 14nm CMOS process. This paper presents the new feature to improve the accuracy and the robustness of the DC offset voltage trimming of the analog components, as an extension of the ADC. DC offset voltage trimming is one of the most common calibration scenarios for the on-die analog components, such as the DC offset voltage trimming of the OPAMP, the analog comparator, the bandgap voltage reference, the on-die linear voltage regulator, etc., in order to reduce the variability in the analog voltage that is produced by the process variation.

2. DC offset Voltage Auto Trimming Hardware for the on-die Analog IPs

Figure 1 depicts the on-die DC offset voltage trimming circuit, together with the on-die analog component under calibration. This trimming hardware is commonly used in industry [2]. There is a resistor divider that converts the tester-given VDD into DC target voltage, which feeds into the analog comparator to be compared with the DC output voltage of the analog component under calibration. The analog component under calibration has an embedded digital-to-analog converter (DAC) internally, so that the DC output voltage can be adjusted up and down by changing the trim code. The implementation is such that the DC output voltage gets higher with higher trim code, and vice versa. Based on the comparison, the up/down counter is incremented or decremented, and eventually, the DC output voltage from the analog circuit is getting converged to the target value.

Figure 2 shows the proposed on-die analog voltage measurement circuit, together with DC offset voltage trimming circuit. The feature has two different modes of operations: the ADC mode and the trimming mode.

In the ADC mode, it is a regular 10 bit analog-to-digital conversion from the analog voltage for measurement to the digital code, and it is for the production testing of the analog circuits. The relationship of the ADC code with the analog voltage can be written as follows:

$$\text{ADC Code} = \frac{\text{Analog Voltage}}{\text{Reference Voltage}} * 1023 \qquad \textbf{Eqn. (1)}$$

In the trimming mode, the operation is similar to the approach that was introduced as Figure 1, but the comparison is executed in the digital domain. The feedback based on the up/down counter is almost the same as that in Figure 1. In this mode, rather than operating as a10 bit ADC, it operates as a 6 bit ADC to reduce the conversion time, and the derived 6 bit code is compared with the target DC voltage (6 bit digital code). The target DC voltage is specified by the 6 bit digital code that can be written by the following equation:

$$\text{Target Code} = \frac{\text{Analog Target Voltage}}{\text{Reference Voltage}} * 63 \qquad \textbf{Eqn. (2)}$$

Figure 3 describes the operation of the backend digital decimation filter. In the ADC mode, it is a regular accumulate / dump digital filter. In the trimming mode, it is a designed such that the quantization error for the previous comparison that is stored in the integrator capacitor can be carried into the next comparison without degrading SNR, due to the noise shaping, and it enables the ENOB of substantially better than 6 bits up to ~10 bits for the accuracy, in spite of using a 6 bit ADC.

3. Evaluation of the Auto Trimming Circuit based on the silicon measurement

Figure 4 shows the distribution of the DC output voltage of

the voltage reference circuit before the auto trimming, while Figure 5 shows that after the auto trimming. The data are based on the measurement of 10731 silicon units that were manufactured on 14nm CMOS. For the trimming operation, the target DC voltage was set to about 0.463 V. Before trimming, the mean voltage was around 0.398 V that was much lower than the target, and the variability was about 27.5 mV for 1 sigma. After the trimming, the mean voltage was converged to the target voltage, 0.463 V, and the distribution was roughly 3.17 mV for 1 sigma. Based on the measurement of 10731 units, the worst case error turned out to be only +/- 11 mV after auto-trimming.

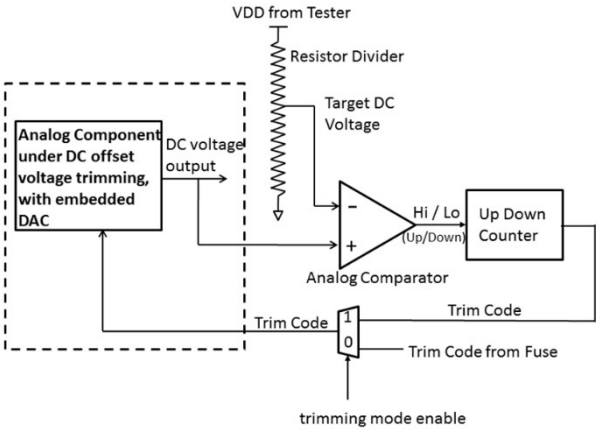

Figure 1: Hardware that is commonly used for DC offset voltage trimming of an analog circuit

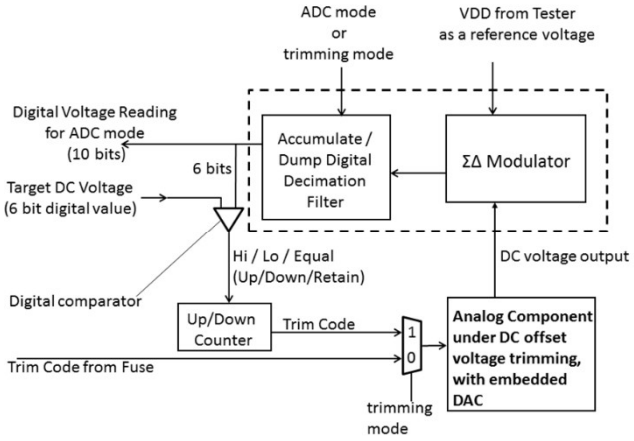

Figure 2: Proposed Analog DFT solution based on the analog voltage measurement circuit, together with the embedded DC offset voltage trimming circuit for analog components

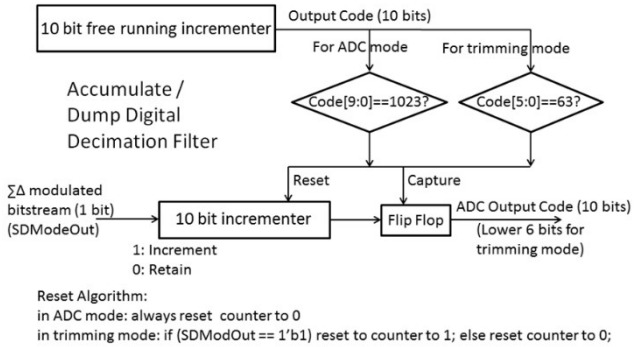

Figure 3: Detailed view of Accumulate / Dump Digital Decimation Filter and its functionality

4. Conclusion

The ADC for analog DFT, together with the new auto trimming circuit for the DC offset voltage has been presented, which is robust enough to be used for HVM. With only a minimal silicon area increase, this new functionality has been added on top of the ADC. The functionality and the performance of the feature has been verified based on the silicon measurement of 10731 units that were manufactured with 14nm CMOS.

References

[1] Takao Oshita, et al., *IEEE J. Solid-State Circuits*, vol. 51, no. 2, pp. 378-390. Feb. 2016

[2] Morimoto, et.al., *Jpn. J. Appl. Phys.* Vol. 51, 02BE, pp10-1 – 10.6, (2012)

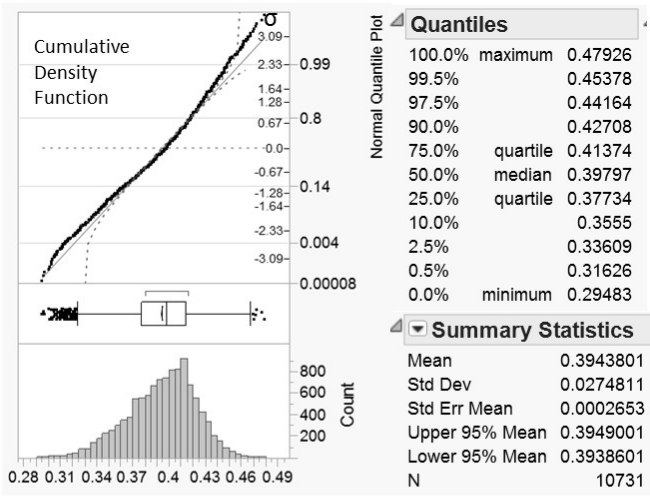

Figure 4: Distribution of DC output voltage from Voltage Reference Circuit *before* DC offset voltage trimming (Measured)

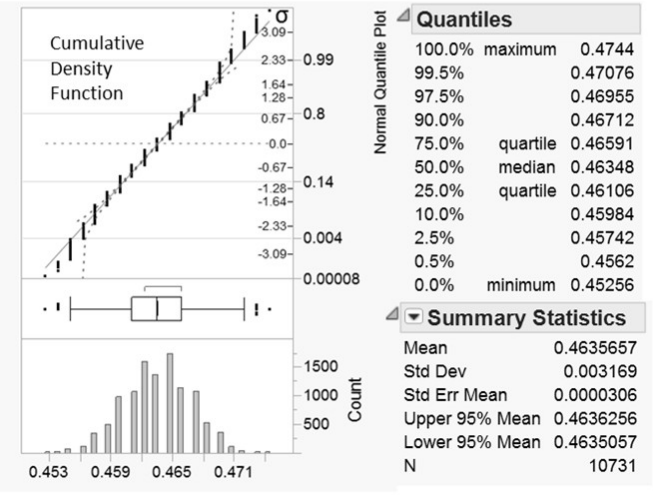

Figure 5: Distribution of DC output voltage from Voltage Reference Circuit *after* DC offset voltage trimming (Measured)