Extended Abstracts of the 2017 International Conference on Solid State Devices and Materials, Sendai, 2017, pp351-352

G-8-03

A 120dBΩ 16MHz Pseudo Differential CMOS Analog Front End Circuit for Optical Probe Current Sensor

Takaharu Uekura, Kousuke Oyanagi, Makoto Sonehara, Toshiro Sato, and Kousuke Miyaji
Electrical and Computer Engineering Division, Department of Engineering, Shinshu University.
4-17-1 Wakasato, Nagano-shi, Nagano, 380-8553, Japan, E-mail: {16w2011g, kmiyaji}@shinshu-u.ac.jp

Abstract

A pseudo differential analog front end (AFE) circuit for a novel optical probe current sensor for high frequency power electronics is designed in 0.18μm standard CMOS technology. The AFE circuit achieves high bandwidth by separating large input photodiode capacitance from the transimpedance amplifier input. The measured transimpedance gain is 120dBΩ and -3dB bandwidth is 16MHz.

1. Introduction

Non-contact and high bandwidth current sensing is essential for advanced high frequency power electronics. The optical probe current sensor (OPCS) using magneto-optic Kerr effect has been proposed as one of the non-contact current sensors [1,2]. In comparison with a conventional Hall- effect current sensor with magnetic yoke, the OPCS has better temperature characteristics, higher electromagnetic noise tolerance, and lower heat generation [1-3]. However, in the previous work, -3dB bandwidth of the sensor is limited to 1MHz due to the analog front end (AFE) circuit [1]. In this work, a 16MHz high bandwidth AFE for OPCS is designed and implemented by 0.18μm CMOS technology.

2. Architecture of OPCS

The structure of OPCS head and the block diagram of OPCS are shown in Fig. 1 and Fig. 2 [1,2], respectively. A magnetic film is placed on top of the target current bus bar and its magnetization direction is set to parallel to the bus bar direction when there is no measured current (I_{meas}=0A). As I_{meas} increases, the magnetization direction rotates according to the magnetic field created by I_{meas}. Besides, circular polarized laser light is irradiated to magnetic film. If the magnetization is rotated by I_{meas}, the polarization of the reflected light also rotates by magneto-optic Kerr effect. The reflected light goes through the half wave plate and polarizing beam splitter (PBS) and divided into P- and S-polarized light, which are received by two photodiodes (PD) to obtain differential current signal i_P-i_S. The AFE circuit finally converts and amplifies the current signal to voltage signal. Table I summarizes the performance of OPCS head. The differential light intensity P_P-P_S ranges within ±1μW corresponding to the linear magnetic field range of ±16kA/m [1,2]. The DC common mode light intensity P_{CM} is 300μW [1,2]. Assuming PD sensitivity of 0.6A/W, i_P-i_S range and the DC common mode current I_{CM} are ±0.6μA and 180μA, respectively.

3. Circuit Design

The schematic diagram of the pseudo differential AFE circuit is shown in Fig. 3. PDs are stacked to remove I_{CM} and pseudo differential scheme is adopted to remove common mode circuit noise. This is effective to remove noisy I_{CM} sink transistor when fully differential scheme is used. The input current signal is converted to differential voltage signals by the transimpedance amplifier (TIA) and then amplified by post-amplifiers. The DC offset cancellation (DCOC) loop corrects differential offset which is induced by the input offset voltage of the amplifiers and the drift of the PD characteristics. In order to realize high bandwidth in TIA, large input capacitance, which is mainly the junction capacitance of the PD, is separated from the TIA input by inserting regulated cascode (RGC) amplifier stage [4] as shown in Fig. 4. The RGC amplifier stage consists of the common gate input stage and common source stage that is used for enhancing g_m of M_1. Common mode feedback (CMFB) loop is added to force the common mode output voltage of the RGC amplifier (V_{CM_RGC}) to V_{CM} by tuning the common mode output voltage of the DCOC amplifier. This assures V_{CM_RGC} to be within the input common mode voltage range of TIA.

4. Measurement Results

The AFE circuit is implemented in 0.18μm standard CMOS technology. The chip microphotograph is shown in Fig. 5. The circuit takes up 870×430μm^2. The measurement frequency responses are shown in Figs. 6(a)-6(d). The transimpeadance gain is 120dBΩ and -3dB bandwidth is 16MHz. CMRR and SFDR are 44dBΩ and 40dB at 100kHz, respectively. The input referred current noise power spectrum density is 0.42pA/√Hz at 1MHz. Fig. 7 shows measured waveforms of the step response. 20ns rise/fall time is achieved. The performance of AFE is summarized in Table II.

5. Conclusion

A pseudo differential AFE circuit for OPCS has been proposed and implemented in 0.18μm standard CMOS technology. It achieves high bandwidth by separating large input capacitance from the TIA input. Compared with the AFE in previous OPCS work, the proposed AFE circuit bandwidth is improved to 16MHz.

Acknowledgement

This work is partially supported by Japan Science and Technology Agency (JST) Kyoto Super Cluster Program and VLSI Design and Education Center (VDEC).

References

[1] K. Ogawa et al., *SSIS*, vol.5, no.2, pp. 347-361, 2012.
[2] D. Karasawa et al., *IEEE Sensors*, pp.1928-1931, 2014.
[3] H. G. Kim et al., *J. Power Electron.*, vol. 9, pp.68-73, 2009.
[4] S. M. Park et al., *IEEE JSSC*, vol.39, pp.112-121, 2004.

Table I Performance summary of OPCS sensor head [1,2].

Measurable maximum current	~600A
Linear magnetic field	from -16kA/m to 16kA/m
Photodiode sensitivity	0.6A/W
Differential light intensity P_P-P_S	±1μW
Differential current i_P-i_S	±0.6μA
Light intensity common mode P_{CM}	300μW
DC common mode current I_{CM}	180μA
Thermal coefficient	0.03%/degC

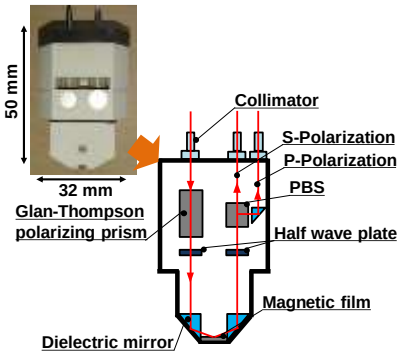

Fig. 1 Structure of the OPCS head [2].

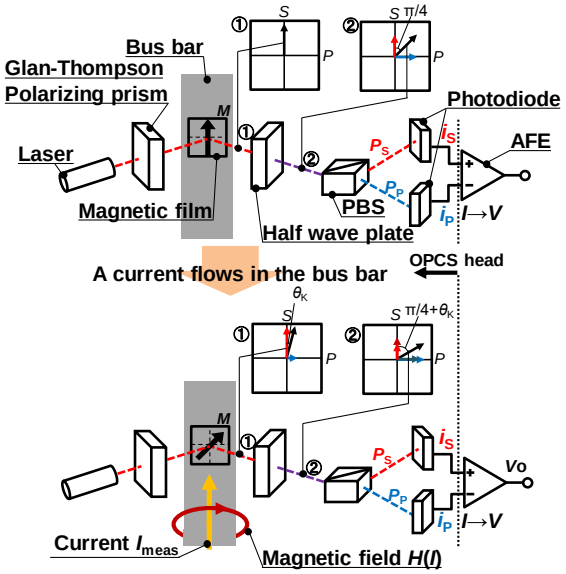

Fig. 2 Block diagram of the OPCS head [1,2].

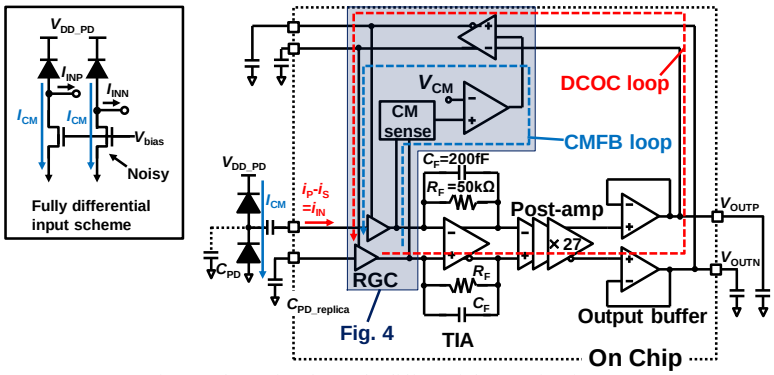

Fig. 3 Schematic of pseudo differential AFE circuit.

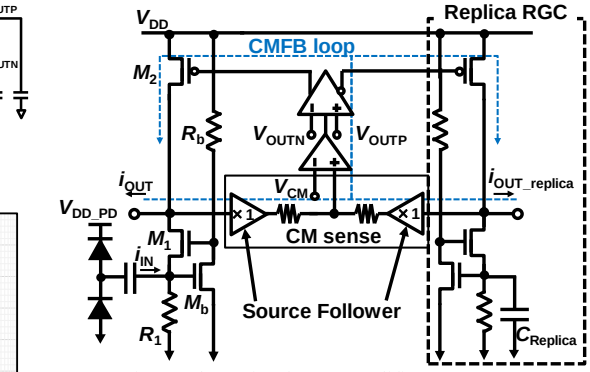

Fig. 4 Schematic of RGC amplifier stage.

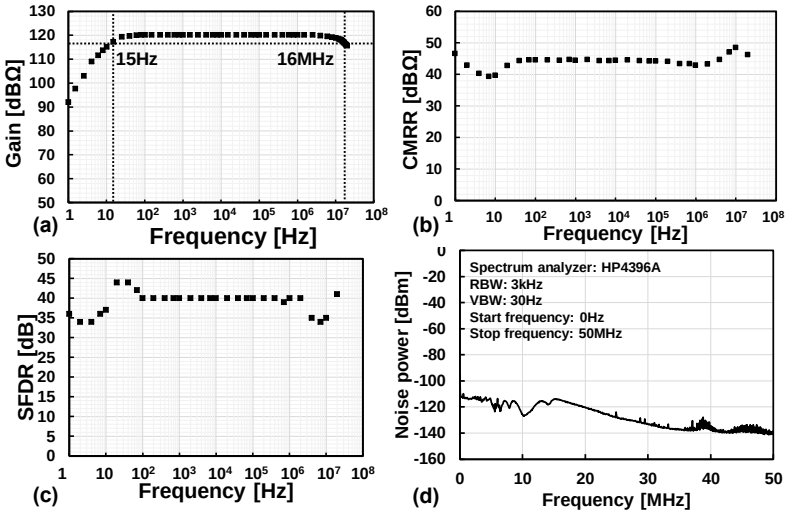

Fig. 6 Measured frequency response. (a) Gain (b) CMRR (c) SFDR (d) Noise power.

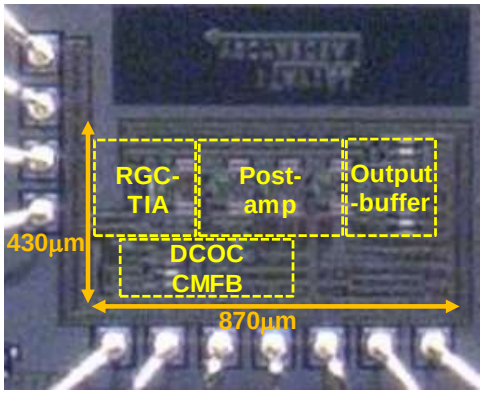

Fig. 5 Chip microphotograph.

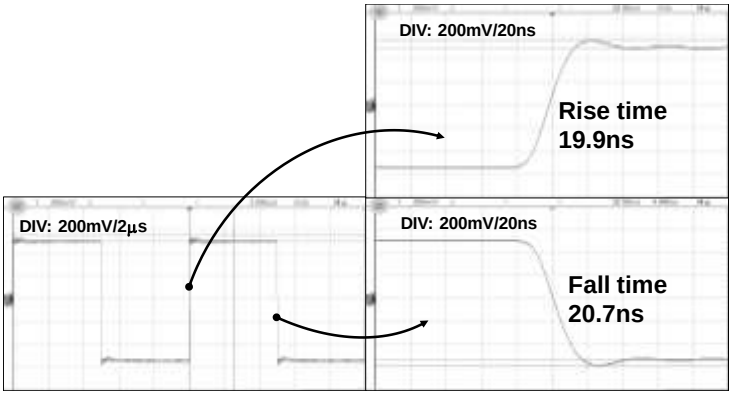

Fig. 7 Measured V_{OUT}.

Table II Performance summary.

Supply voltage	1.8V
Process	0.18μm standard CMOS
Bandwidth (-3dB)	16MHz
Transimpedance gain	120dBΩ (differential)
SFDR	40dB (100kHz)
CMRR	44dBΩ (100kHz)
Input current referred noise	0.42pA/√Hz (1MHz)
Photodiode capacitance	7pF (3.5pF×2)
Power consumption	23mW
Input current	±0.6μA
Chip area	870 × 430μm²