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Development of a technology platform using advanced die-first FOWLP for highly integrated flexible hybrid electronics

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Abstract A novel fan-out wafer level packaging (FOWLP) is studied to develop a technology platform for flexible hybrid electronics (FHE). Small dielets are embedded in a biocompatible flexible substrate we call FlexTrate™. These dielets can be communicated through high-density interconnects formed in wafer-level processing. We demonstrate that 625 pieces of 1-mm-sqaure/ 100-μm-thick Si dielets are integrated in a polydimethylsiloxane (PDMS). In this study, 10-μm-pitch die-to-die interconnects are implemented on the PDMS/dielets, and in addition, the integration process is optimized and the resulting FlexTrate™ is characterized for FHE.

1. Introduction

FHE combines the flexibility of polymeric printed substrates with the performance of inorganic crystalline semiconductor devices to create a new category of electronics. In order to enhance the flexibility, typically, extremely thin semiconductor dies are mounted on the FPC (flexible printed circuits) boards. This is because such thinned dies can be more flexible and follow curved structures. However, high stresses are applied to the bended dies.

In our approach, rigid small dielets are embedded in flexible polymeric substrates we call FlexTrate™ which is fabricated at the wafer level using an advanced die-first FOWLP (Fan-Out Wafer-Level Packaging) technology. FOWLP is expected to reduce package sizes and shorten inter-chip wirings [1]. High flexibility is given by the structure of the FlexTrate™ consisting of the hard and soft segments. Thanks to the FOWLP, the FlexTrate™ allows much tighter interconnects compared to conventional printed flexible electronics fabricated in roll-to-roll or sheet-level processing. The great advantage of FlexTrate™ is that wire binding and solder bumping are not required for communicating between neighboring dies and substrates. FlexTrate™ using inorganic semiconductor dielets can realize highly integrated flexible device systems without the use of organic semiconductors.

In this study, we demonstrate fine-pitch (<10μm) interconnect formation on the PDMS in which Si dielets are embedded by using an advanced die-first FOWLP technology. In addition, die shift and coplanarity between PDMS/dielets are characterized to optimize the new flexible device integration processes. From a reliability point of view, the bendability of the FlexTrate™ is also evaluated by repeated bending cycle test.

2. Experimental

Fig.1 shows the total process of FlexTrate™ fabrication. A removable temporary adhesive layer was formed on the 1st Si handler. Then, 1-mm-sqaure Si dielets with a thickness of 100 μm were precisely placed in a face-down configuration on the adhesive formed on the 1st handler. A biomedical grade PDMS (MDX4-4210/Dow) was applied on the die-on-wafer structure, followed by compression mold with the 2nd Si handler having another temporary adhesive layer. The 1st handler was then thermally debonded at 130°C, and subsequently, the hundreds of the Si dielets were transferred to the 2nd handler. Prior to the following metallization processes, a thin stress buffer layer is deposited on the PDMS/dielets. By using standard photolithography processes with a vacuum evaporation technique, fine-pitch Au wirings were formed on the array of the Si dielets and the surrounding PDMS at the wafer-level to interconnect the dielets at fine pitch. Finally, the FlexTrate™ was thermally debonded again from the 1st handler.

3. Results and discussion

As shown in Fig. 2, 625 (25 by 25) pieces of Si dielets are transferred from the 1st handler to the 2nd one. The 3D surface profiles are measured with a surface metrology systems (CT100/cyberTECHNOLOGIES) equipped with confocal white light. As is seen from Fig. 3, the average coplanarity between molded PDMS and transferred dielets are 3 μm or more and almost all dielets shows the die tilt of within 1 μm. These height gaps result from die placement conditions etc. Figure 4 shows the effect of PDMS curing temperature and adhesive thickness on these height gaps. The die tilt, in other word, height gaps of inert-dielets and the coplanarity between PDMS and Si can be reduced down to 1 μm when we employ the room-temperature PDMS curing and 10-μm-thick temporary adhesives. Surprisingly, die shift after curing the PDMS at 25°C exhibits nearly zero even though typical FOWLP processes using rigid epoxies have the serious die shift issues far exceeding 10 μm [2]. This is due to the low Young modulus of PDMS within 0.1 MPa in addition to the low curing temperature. By using surface modification with O_2 plasma (power: 65 W, O_2 flow: 100 sccm, and etching time: 30 sec) on the PDMS, the adhesion between the PDMS and coming stress buffer layer is enhanced. The stress buffer layer formation can allow the subsequent metal deposition without microcracks by mitigating the CTE/modulus/elongation mismatches between the PDMS and metals (10-nm-thick Ti as an adhesion layer and 200-nm-thick Au). As shown in Fig. 5, 10-

μm-pitch Au wirings (L/S of 3/7 μm) are successfully formed on the array of Si dielets and the surrounding PDMS.

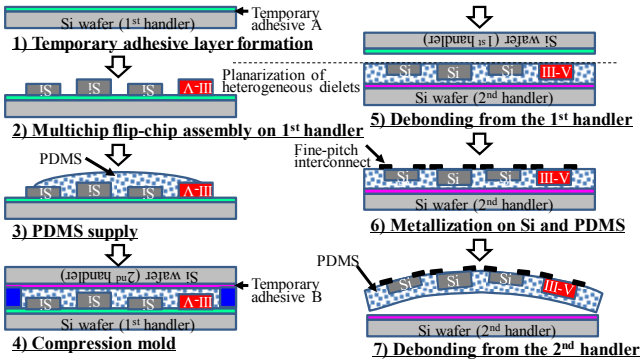

Fig. 1 A FlexTrate™ process flow.

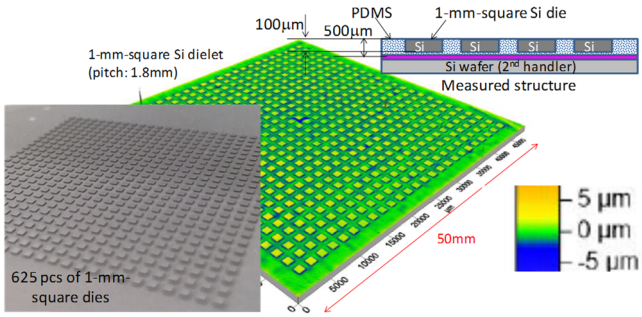

Fig. 2 A photo and 3D surface profile of Si dielets embedded in molded PDMS after transfer to the 2nd handler.

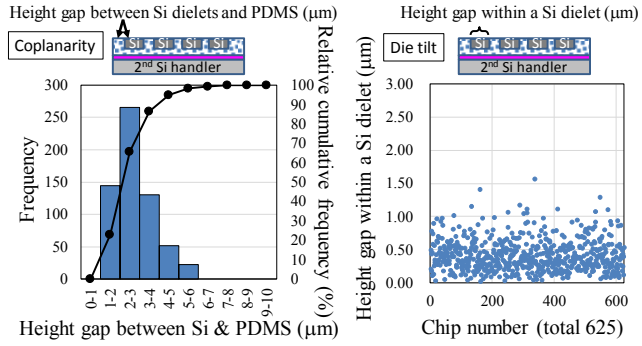

Fig. 3 Coplanarity between PDMS/dielets and die tilt.

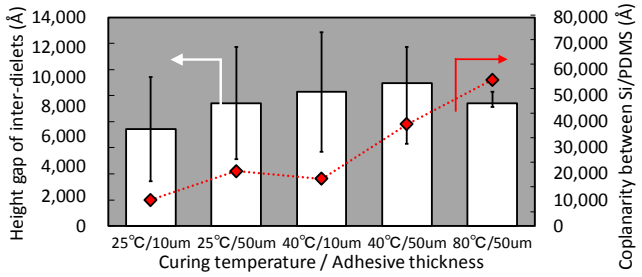

Fig. 4 Impact of PDMS curing temperature and adhesive thickness on height gaps of inert-dielets and between PDMS/dielet.

As shown in Fig. 6(a), excellent linear relationships are obtained by I-V measurement of the fine Au wirings with the minimum wire width of 3 μm. As shown in Fig. 6(b), the resistance formed on the PDMS have high endurance against 1,000 cycle repeated bending test with a curvature radius of 5 mm (DLDMLH-FS/Yuasa). The FlexTrate™ embedding large numbers of the small Si dielets in the PDMS can be attached on the curved surfaces (Fig. 7) such as the human arm and implanted into the human body including the brain.

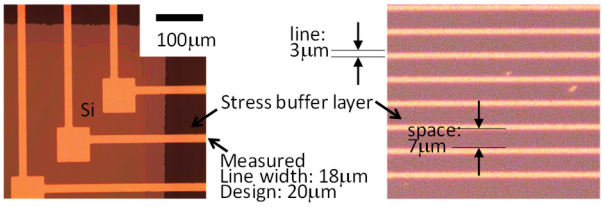

Fig. 5 Photos of fine-pitch Au wirings formed on PDMS/Si.

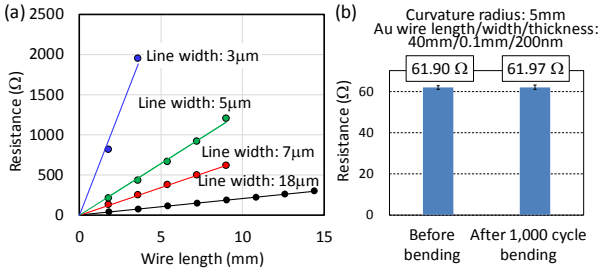

Fig. 6 I-V data of Au wirings formed on PDMS/Si (a) and the resistances before/after 1K cycle bending test (b).

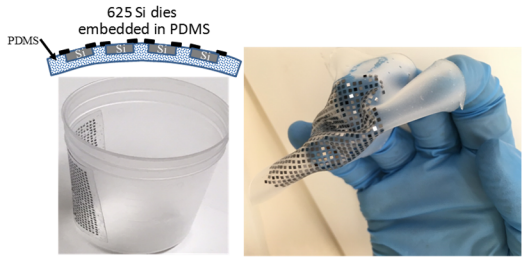

Fig. 7 Pictures of bendable demonstrators of FlexTrate™.

4. Conclusions

We have integrated FlexTrate™ using the new technology platform based on FOWLP for high-performance and scalable FHE. 10-μm-pich Au wirings are successfully formed on the PDMS in which Si dielets are embedded and planarized. The heterogeneous integration scheme can enable next-generation IoT systems having various sensors and high-density interconnects on flexible substrates as well as wearable and implantable devices.

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