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N5 BEOL Process Options Patterning flows Comparing 193immersion to Hybrid EUV or Full EUV

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Abstract

The foundry N5 node requires 16nm half-pitch interconnects for the advanced logic BEOL. Imec has evaluated on testchip vehicles different integration approaches : 193i SAQP (Self-Aligned Quadruple Patterning), LE3 (triple patterning Litho Etch), tone inversion, EUV SE (Single Exposure) with SMO (Source-mask optimization) . Four different patterning combinations have been evaluated to reach this scaling to dual damascene. In this paper, we will compare these process flows and link them to their wafer cost and then recommend a best option.

1. Introduction

The semiconductor scaling roadmap shows the continuous node to node scaling to push Moore's law down to the next generations. 193 immersion conventional patterning schemes are now at their cliffs. Optical immersion usage now requires self-aligned and/or multiple patterning technique combinations to enable such critical dimension. On the other hand, EUV insertion investigation shows that 16 nm half pitch is still a challenge. So, waiting for a full EUV integration scheme for this node, a limited EUV insertion for block cut (aka Tip to Tip, T2T) and vias on top of an SAQP grating can be implemented.

2. Summary

N5 foundry design rules are based on a 42 nm pitch for metal 1 layer and a 32 nm pitch for the next metal 2 layer：
M1 is considered as a dummy layer, 21 nm half pitch single damascene in 40nm SiO2, dielectric. This layer mainly enables the test structures routing for M2/V1.
M2V1 is the 16nm half pitch grating fabricated in 55nm low-k material (k=2.55, porous organo-silicate).
10 nm thick SiCN ensures the dielectric barrier between both metal layers.

Test vehicle mask set allows different combinations of integration. Four different integration flow options for M2V1 16HP have been screened upon process limitations, route complexity and cost. Best patterning flow compromise is then detailed.

Option1 : Tone inversion based on SoC fill and etch back of a storage layer :
7 masks : Core + BLK LE3 + Via LE3
Option2 : Double CMP approach for tone inversion :
7 masks : Core + BLK LE3 + Via LE3
Option3 : Hybrid SAQP 193i and EUV SE :
3 masks : Core + BLK SE EUV + Via SE EUV
Option4 : Full EUV :
2 masks : Metal SE EUV + Via SE EUV

Table I : Design rules for each mask layer,
Develop Inspect Critical Dimension (DICD)
Final Inspect Critical Dimension (FICD)

Layer	Patterning	DICD	FICD
M2 Core	193iSAQP Lines	Line=48nm Space=80nm	Line=16nm Space=16nm
M2 BLK ABC	193iLE3 and tone inversion Holes	41x52nm	LE bias=20nm T2T=21nm
V1 ABC	193iLE3 Holes	41x52nm	LE bias=20nm V1 intrench=21nm
M2 BLK EUV	SE SM0	21x32nm	LE bias=0nm T2T=21nm
V1 EUV	SE SM0	21x32nm	LE bias=0nm V1intrench=21nm
M2 EUV	SE SM0	Line=16nm Space=16nm T2T=25nm	LE bias=0nm Line=16nm Space=16nm T2T=25nm

A : Technical assessment and flow comparison :

Full EUV (option4) because of 16HP Line Space (L/S), tip to tip target and roughness is not process ready yet using current OPC and resist. New iterations including new OPC and alternative resist are being investigated.

SAQP for 16HP L/S (Option 1, 2 and 3) is on the other hand a well know controlled process. It consists of a 2 iterations of Atomic Layer Deposition (ALD) spacer deposition and spacer etch. Process knobs and control are defined from a full factorial DOE to support a pitch walking limited process of record.

Due to the patterning density, 3 colors design is required for the BLK and Via immersion lithography : Overlay control must be tightened. Those immersion options are complex because of the tone inversion needed for the block patterning module :
-The tone inversion based on SoC fill and etch back of a storage layer (option1) is limited due to SoC planarization and mask performance over different features sizes.
-The double CMP approach (option2 : SAQP grating fill with SiO2 / CMP planar / BLK patterned as holes / SiN fill/ CMP planar /SiO2 Selective removal) has been fully demonstrated after fixing several technological challenges (CMP process control, removal of SiO2-material fill selective to SiN-final grating ...). Extra metrology for process control is mandatory.

In the hybrid (option 3), BLK EUV process was set using an innovative Negative Tone Develop (NTD) Metal Containing Resist and a Dark Field (DF) mask, preferred tonality for defectivity. This single exposure process simplification doesn't need the tone inversion. SoC planarization is just required before resist coating. Selected Metal Containing Resist is highly selective to the etch process. Via LE process flow was smartly transferred from imec N10 node module.

In term of process flow for 16HP patterning, Hybrid (SAQP+BLK EUV+Via EUV) is a 39 steps sequence in comparison to the 89 operations needed in the double CMP approach (Fig. 1).

B : Cost per wafers :

Based on the imec cost model, these four flows were evaluated, normalized and compared (Fig. 1, Normalized Process/Module Cost).

Hybrid option 3 shows a significant benefit (~30%) compared to the immersion alternatives due to reduction in total number of process steps. Based on the number of metal layers where we can implement the EUV-based block and via, the impact on wafer cost level could be ~15%.

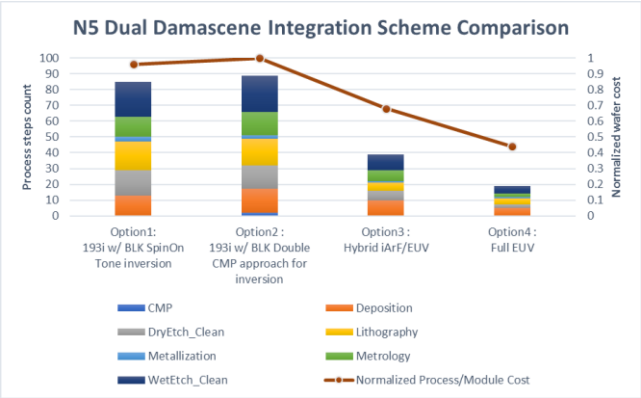

Fig. 1: DD M2V1 patterning options versus integration scheme process step count and wafer cost analysis.
(Trough Put in Wafer/Hour Assumptions:
193i-TP=200 WPH; EUV-TP = 125 WPH)

C : Hybrid flow patterning performance

M2 SAQP patterning process tuning knobs are core1 post etch CD, Spacer1 and Spacer2 deposition thicknesses. In a 48P128 LineSpace structures, 3 different kinds of trenches are patterned and targeted at 16nm : Core defined (CDU $_{\text{across wafer}}$ 3σ = 1.2nm), Gap defined (CDU $_{\text{across wafer}}$ 3σ = 1.8nm), and SP1 defined (CDU $_{\text{across wafer}}$ 3σ = 1.2nm).
M2 Block CD process anchoring was done in a 7.5 track clip that is designed for 5 different lengths of cuts (Fig. 2.b). Transferred in TiN for 21nm tip to tip, only the block width can be measured. Uniformity was averaged on the 5 different kind of block lengths (CDU 3σ $_{\text{across wafer}}$ = 1.3nm).
Via CD performance can only be evaluated and measured at resist level (metrology capability down in lowk). Targeting 21 nm width, reasonable uniformity was achieved : CDU 3σ $_{\text{across wafer}}$ = 1.7nm and LCDU 3σ = 2.2nm.

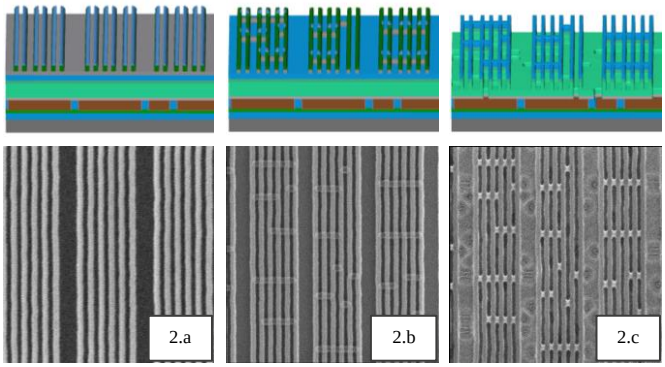

Fig. 2: 7.5 track logic design, M2V1 hybrid patterning.
2.a : M2 SAQP SiN grating 16HP, 2.b : M2 BLK in TiN, 2.c : M2V1 Dual Damascene in lowk

3. Conclusions

16HP Hybrid integration as described (ArFi SAQP + EUV Block +EUV Via) is the most promising option for the first EUV insertion in industry and an sustainable alternative option waiting for the EUV single exposure readiness. The implementation of a Metal Containing Resist (NTD/DF) for BLK EUV Single Exposure has enabled this hybrid configuration.

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