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Advanced Packaging Technology to Address Micro-bump Solder Bonding and Warpage in Large-die 3D IC using 22nm ULK Dielectrics

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Abstract

We discuss recent die level face-to-face 3D IC packaging technology. A micro-scrub bonding process that does not use flux has been evaluated as a potential flip chip bonding method for large IC die with micro-bumps. In addition, an enhanced thermo-compression (TC) bonding process has been developed to address warpage problems when assembling large 3D die on an organic substrate. Challenges related to maintaining co-planarity between thin IC die and laminate substrate were overcome. Large thin IC die (> 600 mm^2) with 22 nm Ultra low-k (ULK) CMOS devices were "3D" packaged.

1. Introduction

Die size for high-end processors and graphics chips can be large X-Y size and require integration. For example, the IBM POWER8, 12-core processor in IBM 22nm silicon-on-insulator (SOI) technology, has a die size of 650 mm^2. Large die 3D IC packaging and heterogeneous integrations can support continuous performance enhancement in Exascale computing systems. Die stack for a plurality of micro-bumps and die warpage control during assembly process are one of the biggest challenges in achieving large die 3D IC packaging [1, 2].

Conventionally flux material is applied to the bonding surface to remove a native solder oxide which prevents solder flow to the surfaces of the corresponding metal pad. After the bonding, a washing process is usually required for removing the flux residue that may result in underfill (UF) void [3]. Removal of flux residue becomes more difficult in the case of 3D IC due to high-density low-height micro-bumps as vertical interconnections existing in the narrow gap between two IC die. The flux residue problem becomes more severe especially for larger die [4, 5]. A micro-scrub TC bonding process was developed as one of the methods to enable flip chip bonding without the use of flux and its associated washing process [2]. Many techniques such as non-conductive film (NCF), non-conductive paste (NCP), and formic acid vapor were suggested as a fluxless bonding method. Nevertheless, the micro-scrub has advantages over others methods since it does not need chemical agents. In the first half of this paper, we discuss a new micro-scrub bonding method.

Another challenge is planarity or warpage control of both thin IC die and laminate substrate during 3D packaging process. Neither thin IC die nor laminate substrate is perfectly flat [6]. As shown in Fig.1, thin IC die are highly warped even at room temperature and the warpage of thin die may change up to 1.5 mm between room temperature and bonding temperature. This is mainly because of the residual stress induced by materials such as thick Cu wiring that is used in back end of the line (BEOL) in CMOS [7]. Unbalance of metal loading in top and bottom of a thin IC die also causes significant warpage [8]. Different warpage behavior between laminate and highly warped thin IC die during 3D IC packaging process may result in solder joint defects such as non-wetting-C4 (Controlled collapse chip connections) and bridging-C4s (Fig.1), and delamination of various interfaces. Due to Coefficient of Thermal Expansion (CTE) mismatch among materials used in thin IC die and laminate, warpage varies with temperature. Furthermore, the effect of warpage becomes more severe in the case of thinner and larger die. Various packaging methods for 3D IC have been proposed, but most of them are for smaller dies and requirements are different compared to high-end processors [9-12]. In the latter half of the paper, we discuss a newly developed 3D IC packaging method addressing the planarity control or addressing warpage issues.

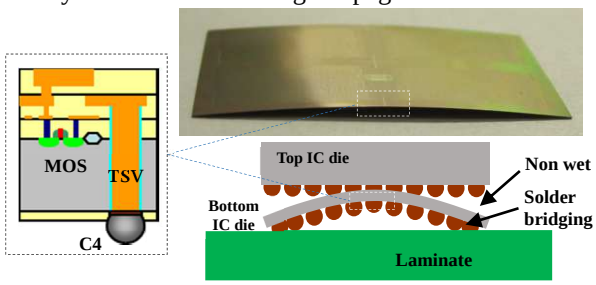

Fig. 1 Warped thin CMOS die causing serious problems to 3D IC packaging.

2. Addressing Micro-bump Solder Bonding

A Micro-scrub bonding process

A micro-scrub bonding process does not need plasma treatment and flux dispensing before TC bonding. Fig.2 shows a micro-scrub process flow. During an alignment process between a top-IC die and bottom-IC die, nitrogen is filled to create an environment of the low oxygen concentration in the specific space where the bonding will occur. Under a specific force, a micro-scrub action is applied to the direction that is perpendicular to the direction of the bonding force, to break up the native oxide layer of a surface of the SnAg solder micro-bump. TC bonding head and stage maintain a coplanarity between the top-IC die and the bottom-IC die during bonding process. A bonding system was designed and developed to achieve the unique process mentioned above and to avoid damage to the IC or connection.

Bonding Results

A test vehicle with more than 170000 micro-bumps was used for evaluation of the micro-scrub bonding process. The size of the test vehicle is bigger than 600 mm^2. The top die consisting of 20-µm Cu /15-µm SnAg micro-bumps was bonded to Ni/Au pads with 61 µm pitch on the bottom die with optimized parameters for a micro-scrub bonding process. Fig. 3 shows cross-sectional SEM images of a sample after bonding with and without micro-scrub process. Fig.3(a) shows solder wettability problems of a solder joint without micro-scrub while Fig.3(b) shows properly joined micro-bump with micro-scrub. Through SEM and Energy Dispersive X-ray Spectroscopy (EDS) observations, a sufficient amount of inter-metallic compounds were confirmed at the bonding interface (Fig.3(c)). The experiments exhibited excellent micro-bump solder joints by using a micro-scrub process that improves the wettability of the solder.

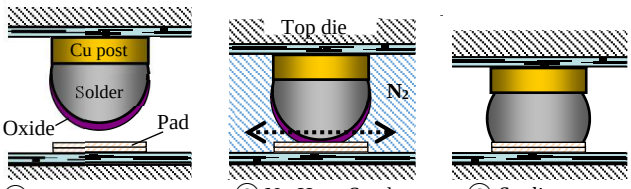

Fig. 2 Process flow of a micro-scrub bonding.

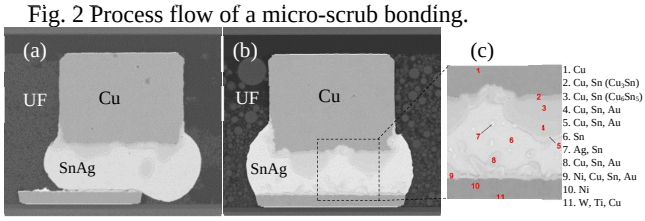

Fig. 3 Cross-sectional SEM image of micro-bump (a) without micro-scrub, (b) with micro-scrub, (c) EDS result.

3. Addressing Die Warpage

An Enhanced Thermo-compression bonding process

The new assembly method was developed to overcome warpage challenges originating in the process of large die 3D integration. A vacuum distribution plate consisting of a plurality of holes that matches C4s of the bottom-IC die was made. The bottom die is placed on the plate such that C4s of warped bottom-IC die are aligned with the holes in the plate. The C4 side of the bottom die is vacuumed through the holes of the plate so that the warped bottom die is kept flat during the subsequent bonding process between top die and bottom die. The IC die stack is then removed from the plate after the bonding by releasing the vacuum. This IC die stack can be subsequently bonded to a laminate by using a belt furnace. Fig. 4 shows optical microscope images of large-die 3D IC that was assembled by using this method.

Characterization

Fig. 5(a) shows cumulative probability distribution of electrical resistance of interconnection that includes Cu TSV, SnAg micro-bump, BEOL wiring, C4, and laminate wiring. Two different micro-bump geometries at 61 µm pitch and at 131 µm pitch were evaluated and the measurement results of 7 samples for each were shown. The figure shows a tight distribution of electrical resistance among the samples for each geometry. The results indicate that the 3D bonding and assembly process was reliable to achieve high-quality connections. In addition, changes in thermal resistance at interfaces in packaged 3D IC were monitored as a part of the reliability test. Thermal sensors were embedded in the BEOL layer in the assembled 3D IC to monitor the efficiency of heat transfer at the die-to-die interface (Rd-d) in deep thermal cycling (DTC) (-55ºC to +125ºC). The heat generated in bottom-IC die must transfer through the interface consisting of two level of BEOL Cu, micro-bump, and UF into the top-IC die to the outside of the package. The thermal resistance of the interface from the top-IC die to the lid through a thermal interface material was also monitored (Rint). Results showed a stable thermal resistance of both Rd-d and Rint through 1500 cycles DTC testing (Fig.5(b)).

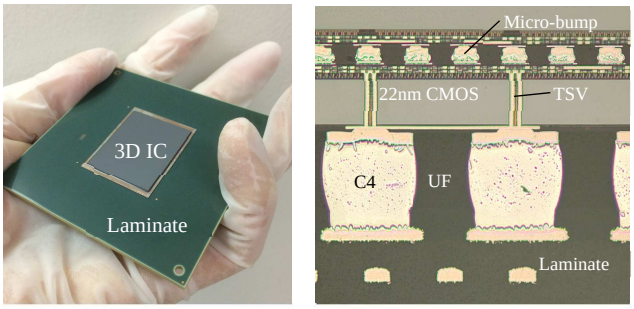

Fig. 4 Large-die 3D IC using 22nm ULK dielectrics (a) after assembly, (b) Cross sectional image.

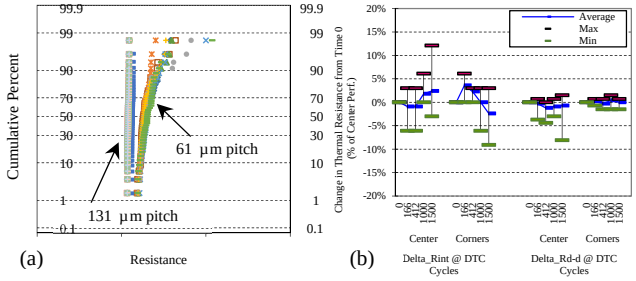

Fig. 5 (a) Resistance measurement over for 3D module, (b) Thermal reliability of TIM1 and die-to-die interfaces.

4. Conclusions

We have presented here a brief overview of challenges of 3D IC packaging and summarized newly developed assembly technologies such as Micro-scrub bonding and Enhanced TC bonding. The proposed technologies have the opportunity to be the candidate used for large 3D IC for Exascale computing and large heterogeneous component integration.

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References

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