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Evaluation of Substrate Noise Suppression Method to Mitigate Crosstalk among TSVs

Yuuki Araga[1], Katsuya Kikuchi[1], Masahiro Aoyagi[1]
[1] NeRI, National Institute of Advanced Industrial Science and Technology, AIST, Japan

Abstract

Substrate noise from a single through silicon via (TSV) and noise attenuation effect by substrate tap or guard ring is revealed by silicon measurement. A CMOS test chip is designed and 6 μm diameter TSVs are manufactured on the 20 μm thickness silicon with via-last method. On-chip waveform evaluation circuitry is embedded on the test chip to capture transient waveform of the substrate noise.

Experimental results show increased substrate noise level by TSV and effectivity of the substrate tap and guard ring for mitigation of crosstalk among TSVs.

1. Introduction

Recent advances of integration technology enabled three-dimensionally integrated LSIs (3D-LSIs). 3D-LSIs consist of multiple tiers of LSIs with through silicon vias (TSVs) on their substrate to allow vertical power and signal transfer among the LSIs. The vertical chip-chip signal transfer by TSVs are considered to enable more energy efficient and wider bus bandwidth compared to conventional wirebonding based signal transfer [1].

On the other hands, a voltage level in TSV and Si substrate around it mutually affect each other because TSV conductor and Si substrate have capacitive coupling through dielectric layer. This mutual affect can cause TSV-TSV crosstalk that loses signal integrity.

In this research, we reveal the level of substrate noise from TSVs by measurement to estimate crosstalk level in 3D-LSIs. We also show effectivities of some considerable substrate noise suppression technique by stabilizing substrate voltage like substrate tap or guard ring, for strategic design to avoid signal integrity degradation [2].

2. CMOS test vehicle with TSV

Figure 1 shows a test structure to capture substrate noise leak out from a TSV. The test chip is designed and manufactured by 0.18 μm CMOS process. After the CMOS process completion, the wafer is flipped and thinned down to 20 μm Si thickness for TSV formation. A diameter of Cu conductor is 5 μm and liner SiO_2 thickness is 0.5 μm. 4 patterns of test structure are shown in Fig. 2. The first 2 patterns including (a) No TSV and (b) TSV are to measure the effect of a TSV on the level of substrate noise. The rest 2 patterns including (c) guard tap and (d) guard ring are for comparison with (b) TSV to evaluate substrate noise suppression effectivity. Guard tap is 2 × 2 μm^2 square shaped substrate tap area, and guard ring is 0.5 μm width substrate tap area surrounding the TSV. The both substrate tap is connected to off-chip ground.

There are 4 measurement points in each pattern, named as

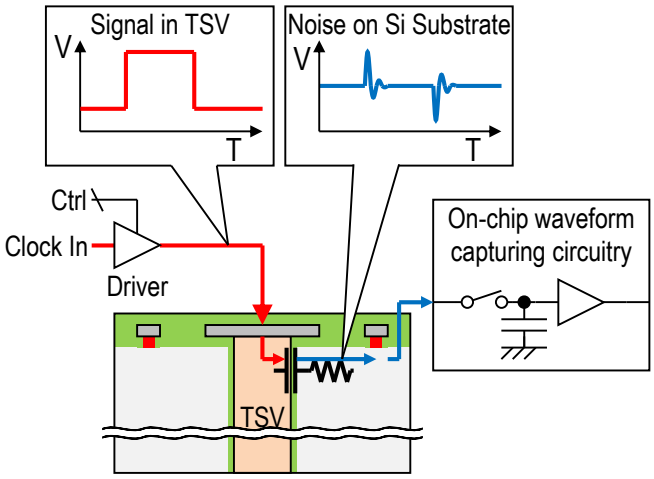

Fig.1. Test structure diagram.

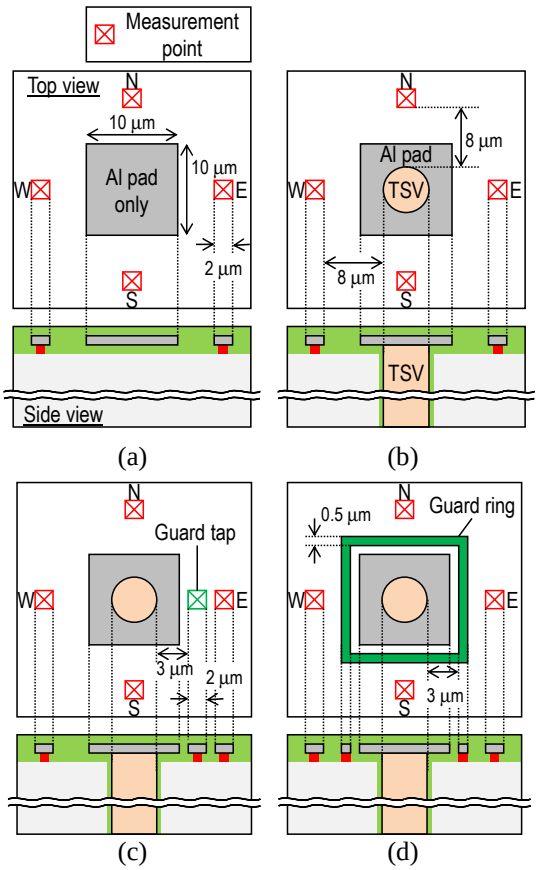

Fig. 2. 4 patterns for substrate noise evaluation. (a) No TSV, (b) TSV, (c) guard tap, and (d) guard ring.

N, W, E, and S point by their positional relation to the TSV. Measurement point is 2 × 2 μm^2 substrate tap and a distance between outer edge of TSV and measurement point is 8 μm.

The measurement points are connected to on-chip waveform evaluation circuitry. It can capture voltage level by

sample-hold circuitry and output to off-chip as current. An off-chip analog-digital converter digitizes the current and a PC stores the digital data. Iterative operation of the procedure enables capturing transient waveform of the target.

3. On-chip measurement

To evaluate noise leakage from TSV, 20 MHz clock signal is introduced to TSV through driver circuitry and excited substrate noise is measured. Figure 3 compares substrate noise level measured at N point, without and with TSV. The plot shows positive and negative noise induced by rise and fall edge of clock signal, respectively. The comparison shows increased substrate noise level by TSV formation, due to larger capacitive coupling.

Noise suppression effect comparison at measurement point N is shown in Fig. 4. In the plot, the guard ring case shows best noise suppression effect, and smaller noise suppression effectivity of the guard tap case is also shown.

Figure 5 shows peak-peak voltage measured at 4 measurement point in each test pattern. Noise level increment from the no TSV case in percentage is shown above the TSV case graph, and noise level reduction from the TSV case in percentage is shown above the guard tap and guard ring case graph. The graph of the guard tap case at the point E shows large noise reduction effect as well as guard ring.

From these evaluations, we can say even a single TSV increases substrate noise which causes crosstalk among TSVs. As for substrate voltage stabilizing method, noise suppression effect at a particular point by guard tap is shown, as well as good noise reduction characteristics of guard ring.

4. Conclusions

Substrate noise from TSVs may cause crosstalk in massive signal transfer paths in 3D-LSIs. The substrate noise is evaluated through real Si measurement and the result shows that larger noise leakage occurs in a case of TSV existence. Guard tap and guard ring are also evaluated as noise suppression methods and good characteristics are also shown. These methods can be used for strategical noise suppression desgin to keep signal integrity.

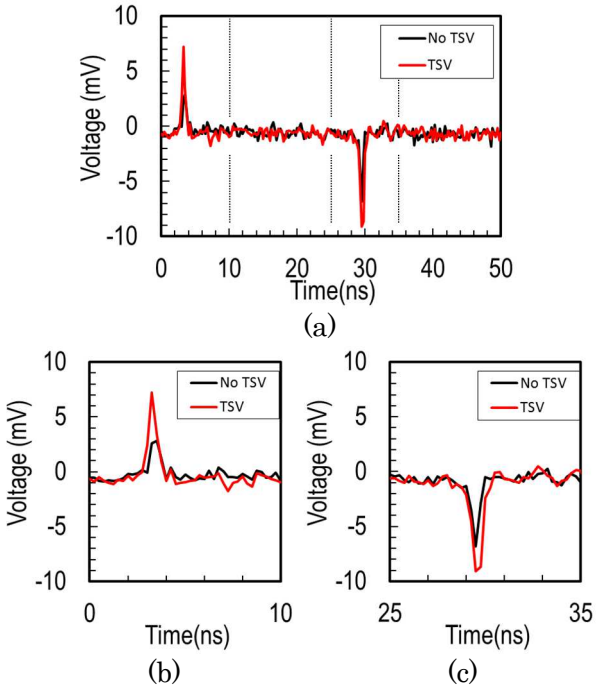

Fig. 3. (a) Measured waveform of no TSV and TSV pattern, (b) expanded plot of clock rise noise and (c) clock fall noise.

Acknowledgements

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References

[1] S. Takaya et al, ISSCC 2013

[2] J. Cho et al, IEEE CPMT symposium 2010.

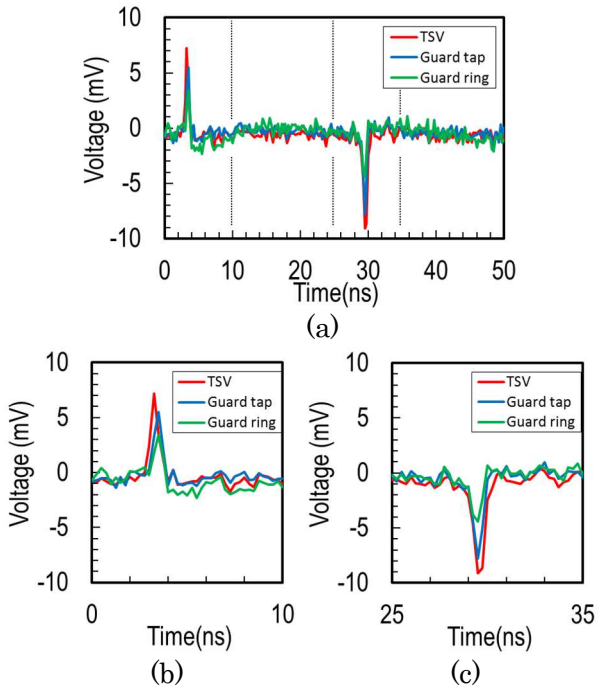

Fig. 4. (a) Measured waveform of TSV, guard tap and guard ring pattern, (b) expanded plot of clock rise noise and (c) clock fall noise.

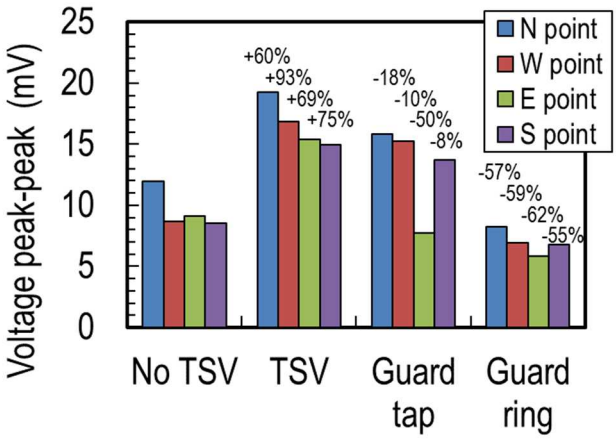

Fig.5. Voltage peak-peak value plot of 4 measurement points in each pattern.