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Characterization of Cu-TSVs Fabricated by a New All-Wet Process

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Abstract

Cu-TSVs were fabricated in high-aspect-ratio Si trenches using a new all-wet process with vacuum-assisted spin-on liner dielectric formation and electroless seed layer deposition. The step-coverages of a spin-on polyimide liner dielectric and an electroless plated Cu seed layer were much higher than those of conventional plasma CVD SiO2 and sputtered Cu. Electrical properties of the Cu-TSVs after bottom-up Cu electroplating were characterized. The measurement results showed that the Cu-TSVs has low capacitances about 32 fF (minimum), low leakage current of 8.3 pA at 20 V, and less influence of Cu contamination, which indicates that the Cu-TSVs formed by the all-wet process can be used for highly reliable 3D-LSI fabrication.

IndexTerms - Electroless plating; spin-on polyimide liner; all-wet process; TSV; 3-D LSI.

1. Introduction

To meet the demands for higher bandwidth, faster data transmission, and lower power consumption, TSVs with-higher density are strongly required for 3-D LSIs. To realize the advantages of increased bandwidth and reduced power consumption through the TSVs in high volume production, TSV's dimension is required to be with smaller diameter and higher aspect ratio [1]. According to the conventional processes for high-aspect-ratio TSV formation, there are some limitations in passivation and metallization because of inherent poor step coverage capability based on PECVD and sputtering technology, respectively. It is essentially necessary to achieve low temperature processes for passivation and metallization with low cost. In this study, we proposed a new all-wet Cu filling process using electroless plating to form a seed layer on the surface of spin-on polyimide liner. Furthermore, we evaluated the electrical properties of the fabricated TSVs and evaluated the influence of Cu contamination from the Cu TSV on device reliability.

2. Experimental

Fig.1 shows the schematic fabrication flow for the all-wet TSV fabrication process. First, high-aspect-ratio (HAR) and high-density blind via arrays were fabricated through deep reactive ion etching (DRIE) on P-type <100>silicon wafers, as shown in Fig.1(a). Then, as shown in Fig.1(b), polyimide PIX-1400(HD microsystems, Japan) was applied for liner deposition of TSV with the vacuum-assisted spin-coating approach [2,3]. Next, the polyimide surface was then etched to promote surface texture, thus enhance the adhesion of Cu, using TMAH (25%) for 5 minutes at room temperature. After that, the substrates were pre-treated and activated at 35°C, followed by a reduction process. The electroless plating process was done in a bath at 35 °C for 10-mins deposition time. The resulting microstructures of the electroless Cu layer were shown in Fig.1(c) and (e). Finally, electroplated Cu is fully filled in the deep Si trenches by the bottom-up deposition at room temperature [4], followed by Cu CMP and patterning, as shown in Fig.1(d). The cross-sectional views of TSVs were observed by SEM. Electrical properties of the fabricated TSVs were evaluated by I-V and C-V measurements with Keysight B1500A at room temperature. Moreover, C–t analysis was also applied to characterize the influence of Cu contamination from the Cu TSV on device reliability [5].

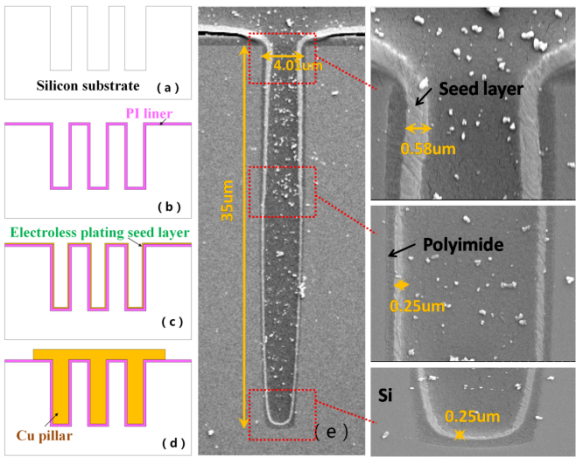

Fig. 1 Schematic TSV fabrication with all-wet processes.
(a) HAR trench etching, (b) vacuum-assisted spin-coating polyimide, (c) electroless plating Cu seed layer, (d) bottom-up Cu filling (e)Cross-sectional SEM of seed layer.

3. Results and Discussions

With the fabrication processes flow illustrated in Fig. 1, spin-on polyimide liner and a electroless Cu seed layer were successfully implemented in 4-μm-diameter/35-μm-depth Si trenches. Fig.1(e) shows the SEM cross-sections of the Cu

seed layer after electroless plating for 10 mins. The resulting thickness varied from 0.58 μm to 0.25μm. Table I lists the

Table I Step Coverages of polyimide liner and seed layer

Position	Polyimide		Cu seed layer	
	Thickness(nm)	Step coverage(%)	Thickness(nm)	Step coverage(%)
Top	1120	-	650	-
Top sidewall	420	37.5	580	89.2
Middle sidewall	250	22.3	250	38.5
Bottom sidewall	450	40.2	245	37.7
Bottom	600	53.6	250	38.5

step coverage distributions along the trench sidewall, with positions at the top surface field, trench top sidewall, 1/2 trench depth, 3/4 trench depth, and trench bottom, indicating better step coverage behaviors than the conventional plasma CVD SiO2 and sputtered Cu. The adhesive force between seed layer and polyimide was proved strong enough for the subsequent Cu electroplating.

Leakage currents from a Cu-pillar through polymer liner to silicon substrate was measured with Keysight B1500A, by sweeping the bias voltage from 0 to 20 V with an increasing step of 200 mV. It can be seen from Fig. 2(a) that the leakage current of TSV was as low as 8.3 pA under 20 V, which indicates good insulation between the Cu TSV and the silicon substrate.

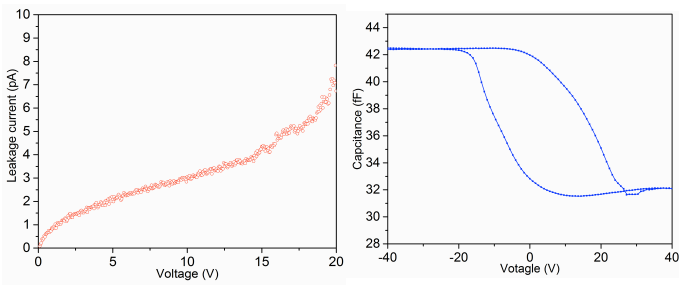

Fig. 2 Electrical measurement results at room temperature.
(a) I-V characteristics of a single TSV, (b)C-V characteristics of a MIS trench capacitor.

The C–V characteristics of the polyimide insulating layer of the trench capacitor was measured using Keysight B1500A at 1 MHz, by sweeping the voltage from –40 to 40 V with an increasing step of 200mV. Fig. 2(b) shows the measured C–V curves of a 35-μm-depth single trench capacitor with the tapered Cu pill arranging from the top diameter of 4.01μm to the bottom of 2.98 μm. The polyimide insulator thickness varied from 600 nm to 250 nm. The minimum capacitance of the trench capacitor was about 32fF, that is approximately half compared to the capacitance for the same size TSV with SiO_2 liner.

To electrically characterize the Cu diffusion from the Cu TSV, the trench MOS capacitor with Cu gate electrode was fabricated. The C–t measurements were performed using Keysight B1500A with sweep voltages from –10 to + 25 V. The C–t curves were plotted as a function of a normalized C/C_f versus measurement time in Fig.3, where C values were measured with a frequency of 1 MHz in the deep depletion condition, C_f was a steady-state capacitance in the inversion conditions, and the transient time t_f was the time required for the capacitance to reach inversion from the initial deep depletion region. The transient time t_f varied as the generation lifetime of minority carrier, which means a longer t_f implies less metallic contamination [6]. The C–t curves show less change from the as-deposition conditions even after annealing up to 30mins at 400°C, indicating that the generation lifetime of minority carriers was not reduced. It means that Cu atoms were difficult to diffuse into the active region owing to the blocking property to Cu diffusion by polyimide liner with the thickness of 250nm.

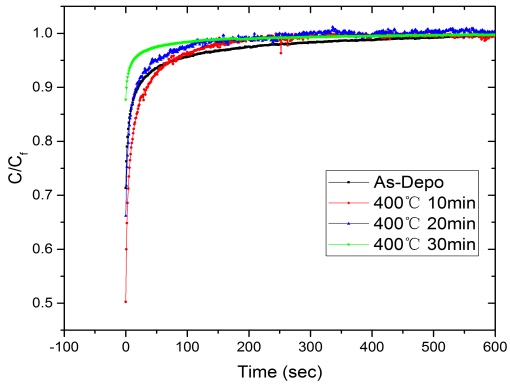

Fig. 3 Measured C-t curves of the trench capacitors after annealing at 400°C and different times.

4. Conclusions

A new all-wet process of TSV filling was achieved successfully by using polymer liner as insulation and barrier layer, and by electroless plating to form continuous Cu seed film at low cost. The good parasitic capacitance characteristics and leakage current properties of fabricated TSVs were acceptable for 3-D integration application. Moreover, C–t measurement results showed that Cu atoms were difficult to diffuse into the active region, which indicates high reliability in the 3-D LSIs.

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