Extended Abstracts of the 2017 International Conference on Solid State Devices and Materials, Sendai, 2017, pp409-410

Fabrication of VTPC-TG Pixels for 3D Structure CMOS Image Sensor Applications

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Abstract

This paper reports the key fabrication processes for a vertical thin poly-Si channel (VTPC) transfer gate (TG) structure, which is one of the candidates for future 3D pixels. The proposed process integration can effectively suppresses the dark current caused from grains of poly-Si in VTPC-TG structured pixel by low temperature solid phase epitaxial growth. Also, the channel punch-through caused from fast dopants diffusion along poly-Si grain was suppressed by unique structure and optimizing drain junction formation processing.

1. Introduction

Driven by the consumer demand for higher resolution sensors, researches of three-dimensional (3D) CMOS image sensor (CIS) have been started [1-3]. We adopted vertical thin poly-Si channel (VTPC) structure which is used in 3D NAND flash memories, and modified to fit CIS pixel applications [4].

However, unlike 3D NAND flash memories, the grain boundaries of poly-Si channel in VTPC-TG pixels act as dark current sources causing image quality deterioration. Until now, effective grain boundary control method of VTPC-TG was not identified. Furthermore, unlike 3D NAND flash cells which are connected in series, TG of CIS pixel is a single transistor having a relatively short channel resulting in vulnerability to channel punch-through.

In this paper, we report the grain boundary related defect suppression mechanism of VTPC-TG for CIS application and the characteristics of dopant diffusion in poly-Si channel depending on process conditions that is essential for manufacturing sub-micron channel length poly-Si transistor.

2. Results and Discussions

Process Integration of VTPC-TG Pixels

Fig. 1 shows TCAD images of both a conventional pixel and the VTPC-TG structured pixel proposed in this study. This new TG structure uses a vertical charge transfer, in contrast with the lateral charge transfer of conventional TG structures. Fig. 2 describes the fill factor increase resulting from the adoption of a vertical channel TG. Conventional TGs are formed in the same process step of the logic transistors and other pixel transistors. However, to fabricate the vertical TG discussed in this study, five additional masks were used after photodiode (PD) formation. Fig. 3 shows cross section illustrations of major process steps for VTPC-TG fabrication.

Fabrication and Epitaxial-Si Growth of VTPC-TG Pixel

Fig. 4 shows images of each steps described at Fig. 3. As shown in enlarged HR-TEM image of PD-to-channel interface area, low temperature deposited amorphous Si was converted to epitaxial-Si. Thanks to the solid phase epitaxial growth (SPEG), grain boundary of poly crystalline channel can be isolated from PD area. Conventional Si-epitaxy requires above 1000 ^{o}C [5]. SPEG, on the other hand, is made at low temperature of around 600 ^{o}C without advanced low temperature EPI-Si equipment. Therefore, we can isolate grain boundaries in poly-Si channel from PD region without changing PD profiles which are formed prior to VTPC-TG.

Dopant Diffusion in the Poly-Crystalline Si Channel

Since dopant diffusivity at poly-Si is several dozen times faster than at single crystal Si [6], it is not easy to fabricate sub-micron channel lengths poly-Si transistor. Fig. 5 shows dopant diffusion lengths differences in single crystal Si and poly-Si substrates depending on RTP conditions. TG requires low leakage and sufficient breakdown voltage (BV) for good image quality. As shown in Fig. 6, even using soak RTP condition, sufficient BV and leakage was successfully achieved. This implies that the dopant diffusion in the thin poly-Si channel is much slower than in the bulk poly-Si structure. Furthermore, unlike TCAD simulation sidewall gate couldn't act as a gate for vertical channel transistor.

3. Conclusions

Replacing the pixel array of an existing 5M 1.12 μm BSI product by VTPC-TG pixels, product-level 5 Mpixel images were obtained. Fig. 7 shows the chip-on-board (COB) module and focused-ion-beam cross section images of the modified BSI test chip. Fig. 8 shows a real photo image obtained with interpolation and auto white balance, but without any other image optimization techniques. Because of the epitaxial growth in the PD-to-channel interface area, the proposed integration process not only effectively suppresses the grain boundary effect. In addition, channel punch-through can be prevented by optimizing the source/drain RTP conditions.

References

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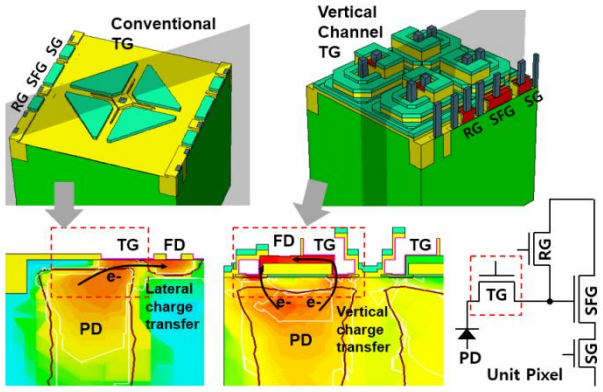

Fig. 1. Comparison of the 3D TCAD images of conventional and VTPC-TG pixels. In this figure, PD, FD, RG, SFG, and SG represent the photodiode, floating diffusion, reset gate, source follower gate, and select gate, respectively [4].

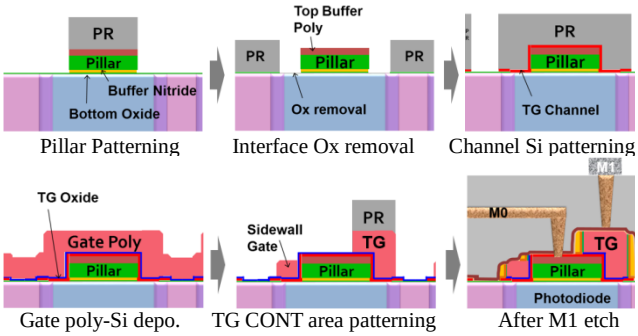

Fig. 3. VTPC-TG fabrication process flow. The bottom nitride in the pillar stack film is used as an etch stop layer, and a top buffer poly-Si is used for the CONT landing buffer layer.

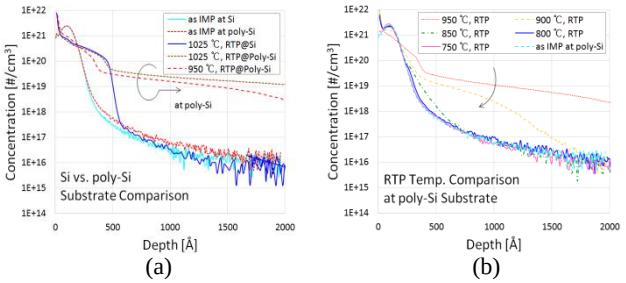

Fig. 5. SIMS comparison results depicting the faster dopant diffusion in poly-Si when compared to that in the Si-substrate, for various source/drain (S/D) formation RTP conditions. Each indicates (a) substrate effect, (b) RTP temperature effect.

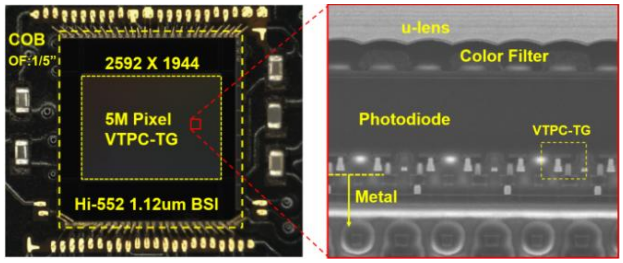

Fig. 7. COB module image of the 1.12-µm, 5-Mpixel, BSI structured, mass production test chip used for characterization, and FIB image of the test chip after VTPC-TG pixel adoption.

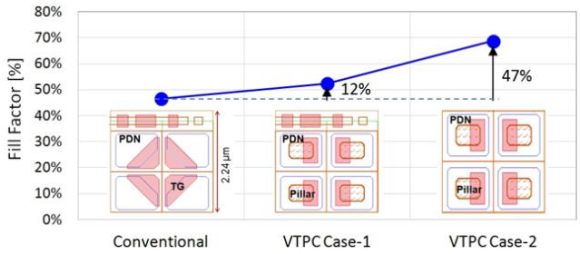

Fig. 2. Comparison of the fill factor (FF) for conventional and VTPC-TG pixels. The FF was calculated using the PD to pixel area ratio; the same type of four-shared pixels were used in the comparison. In this study, Case-1 configuration was used [4].

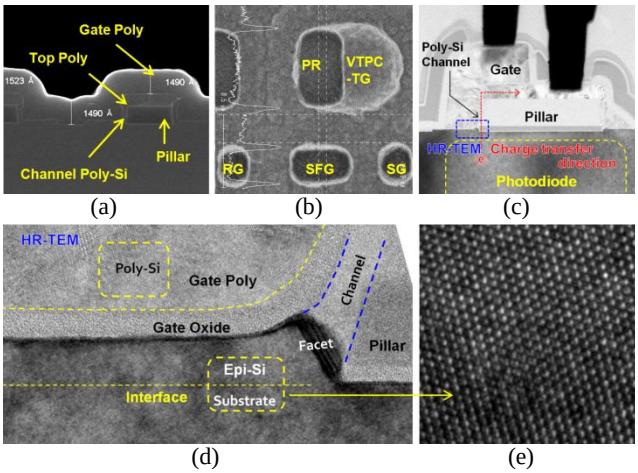

Fig. 4. (a) Cross-section SEM images of gate poly-Si deposition step. (b) Planar SEM image of TG CONT pattering step. (c) TEM image after final processing. (d) and (e) show enlarged HR-TEM image of PD-to-channel interface area depicted epitaxial grown Si.

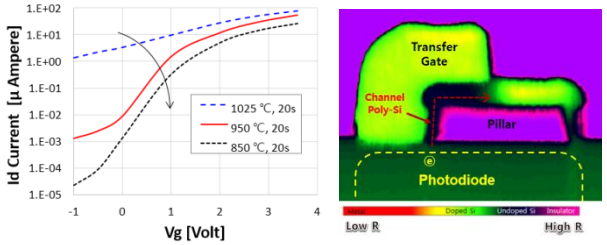

Fig. 6. V_g-I_d characteristics of VTPC-TG depending on soak RTP temperatures. Scanning spreading resistance microscopy (SSRM) image of VTPC-TG indicating dopant activation and less diffusion in thin poly-Si channel than bulk poly-Si.

Item	Description
Sensor Structure	BSI
Test Chip	Hi-552 (Pixel Replace)
Resolution	5M Pixel (2592X1944)
Pixel Structure	VTPC-TG
CFA Type	Bayer RGB
µ-Lens Type	Dual µ-Lens
Operating Voltage	1.2V/2.8V
Pixel Size	1.12 µm
Fill Factor	48.7 %
Integration Time	33 ms
Light Condition	D65

Fig. 8. Example of a 5 Mpixel resolution image captured by the test chip. The VTPC-TG pixels are adopted on a mass-production chip [4].