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Investigation of the effective net charge of strontium silicate layers on silicon substrates at changing annealing condition

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Abstract

We investigated the effective net charge density (Q_{eff}) of strontium silicate (Sr_2SiO_4) film grown on silicon (Si) (100) substrate. Sr_2SiO_4 films were fabricated by pulsed laser deposition using a Sr_2SiO_4 polycrystalline target. And then annealed at 400-600℃ in oxygen atmosphere with a tube furnace. The Q_{eff} values of the Sr_2SiO_4/Si(100) samples were estimated from capacitance-voltage curves. We were obtained the maximum Q_{eff}/q values of $1.03\times10^{13}cm^{-2}$ at the samples with a thickness of 15nm annealed at 400°C. With increasing annealing temperature, the Sr_2SiO_4 layer penetrated into the Si(100) substrate. This penetration may degrade the interfacial properties and decrease the Q_{eff} value of the layers.

1. Introduction

So far, the term "field effect" has been widely used in the field of semiconductor. Especially, the field effect has been widely used as the working principle of field-effect transistors (FETs). This type of field effect can be called an external field effect (EFE) because an external voltage source is required to operate the device. EFE devices have restricted device design because it typically necessary to form electrodes and an external energy source. In addition, because EFE operation required to keep applying bias, it consumes energy.

On the other hand, another type of field effect using statically charged insulator layers have been studied[1]. We obtain static field effect (SFE) without connecting to an external voltage source. Furthermore, they can minimize energy consumption. However, the magnitude of the SFE is limited by the amount of the charges and is fixed after device fabrication. Therefore, it is necessary to design the charge density of SFE layers considering the actual use of the device before fabrication.

In the SFE, the fixed charges (FCs) in the insulator layer usually play an important role, and the magnitude of the SFE increases proportionally with the amount of FC[2]. Thus, controlling the FC density of the charged layer over a wide range is important to tune the SFE. In addition, materials with higher FC density are needed to obtain SFEs of larger magnitude.

Previously, we reported the correlation between the FC state and chemical bonding state of Sr_xSiO_{x+2} thin films fabricated by the reaction of strontium oxide layers on Si substrates[3]. We found that the FC density strongly depended on the amount of Sr_xSiO_{x+2} bonding species (Sr-O-Si) included in the Sr_2SiO_4 films. Thus, we propose using Sr_2SiO_4 as a starting material to obtain layers that exhibit a SFE.

In this study, we investigate the effective net charge density of Sr_2SiO_4 film grown on Si substrate fabricated from a Sr_2SiO_4 polycrystalline target. Furthermore, we measured the FC state and chemical bonding. We also investigate the influence of post-deposition annealing (PDA) on the stability of the Sr_2SiO_4/Si interface.

2. Experiments

p-type c-Si(100) wafers (CZ, ρ=1-10Ωcm) were used as the substrates. All of the Si(100) wafers (size of 0.8×0.8 cm^2) were cleaned by the conventional RCA method and were immersed in 5% HF solution for 1min to remove native oxide layers at the surface. Sr_2SiO_4/Si samples were fabricated by pulsed laser deposition (PLD) using a Sr_2SiO_4 polycrystalline target in a ultra-high vacuum of $<1\times10^{-6}$Pa at room temperature (RT). The thicknesses were from 5nm to 40nm. PDA were done in oxygen atmosphere using a tube furnace. The annealing temperature was 400°C and 600°C. The annealing time was 6 hrs. XPS measurements were performed using an Al Kα hν=1486.6 eV X-ray source in a vacuum below 10^{-7} Pa at RT. C-V characteristics were measured using an LCR meter.

3. Results and discussion

Figure 1(a)-(c) show the C-V curves obtained for the Au/Sr_2SiO_4/p-Si(100)/Au samples with various Sr_2SO_4 layer thicknesses for each PDA temperature. For the sample annealed at 400°C, the accumulation capacitance systematically decreased with increasing Sr_2SiO_4 layer thickness and the flat-band voltage shifted to the negative voltage side. In contrast the C-V curves of the other samples do not behave so systematically. From these C-V curves, we calculated the effective net charge per unit area (Q_{eff}) in the silicate layers. The obtained values divided by the unit charge (Q_{eff}/q) are plotted as a function of sample thickness for each PDA temperature in figure 2. The Q_{eff}/q of all the annealing condition show the same tendency: Q_{eff}/q values rapidly increased with thickness until 15 nm, and then it became constant. At the 15nm-thick sample annealed 400°C, the Q_{eff}/q value was $1.03\times10^{13}cm^{-2}$. This value is of the same order of

magnitude as that reported for an Al_2O_3 layer fabricated by atomic layer deposition on a Si substrate. Figure 2 indicates that most charges are located within 15nm of the substrate surface. This suggests that the optimal thickness of a Sr_2SiO_4 layer as a SFE layer is approximately 15nm.

From the thickness dependence of Q_{eff}/q, we also observed an interesting feature. Figure 3 shoes a magnified view of the thinner layers in figure 2. The Q_{eff}/q value for samples obtained at each PDA temperature increases linearly, as shown by the fit lines obtained by the least squares method. Negative thicknesses were obtained from the intercept of each line on the horizontal axis. The negative thickness systematically decreased with rising PDA temperature. Because the horizontal axis represents the thickness of the deposited layer, the obtained negative thickness indicates the penetration distance into the Si surface. Therefore, we consider that an interfacial silicate-like layer extends into the Si substrates and it becomes thicker at higher PDA temperature.

To estimate the variation of the silicate layer thickness, we conducted XPS measurements of the as-deposited and annealed samples. figure 4(a)-(d) show the observed Si 2p corelevel spectra of the Sr_2SiO_4/Si samples obtained at each PDA temperature. The spectra of the 5 nm samples contain two peaks. The peak at a lower binding energy (BE) of 99.2 eV corresponds to the Si substrate and the other broad peak at higher BE corresponds to the silicate layer on the Si substrate. As the silicate layer thickness increases at the same PDA temperature, the Si substrate peak becomes relatively smaller than the silicate layer peak because of the increased traveling distance of photoelectrons from the Si substrate though the silicate layer. As the PDA temperature rises at the same deposition thickness, the substrate peak also becomes relatively smaller. This peak variation indicates that the silicate layer thickness was increased by PDA. However, the sample thicknesses measured by the stylus profiler did not change before and after PDA. Therefore, this indicates that the increases of silicate layer thickness are caused by penetration of the silicate layer into the Si substrate. And we consider that this migration causes the decrease of the net charge density and degradation of the C-V characteristics of the silicate layers for the samples annealed at 500 and 600°C.

4. Conclusions

We investigated the electrical properties of Sr_2SiO_4 thin films on Si substrates fabricated from a Sr_2SiO_4 polycrystalline target y PLD. The C-V curves of samples annealed at 400°C changed systematically with sample thickness. This indicates that high-quality samples were obtained. The effective net charge density per unit area reached $1.03\times10^{13}cm^{-2}$ for the sample with a thickness of 15nm. This effective net charge density is at same level as that of the Al_2O_3 layer.

Acknowledgements

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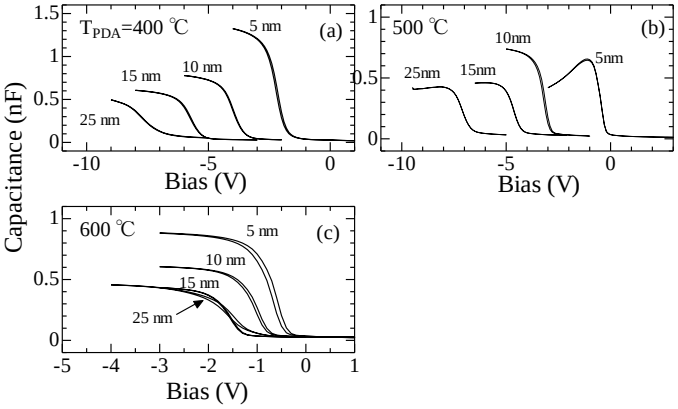

Fig.1 The C-V curves of the Au/Sr_2SiO_4/p-Si(100)/Au samples annealed at (a)400°C, and (b)500°C, and(c)600°C

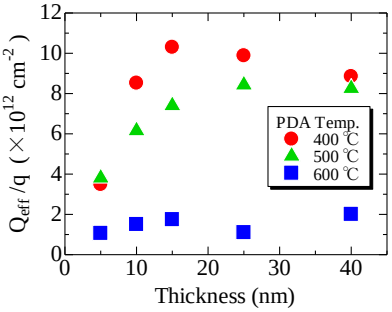

Fig.2 Thickness dependence of the Q_{eff}/q of Sr_2SiO_4/Si(100)

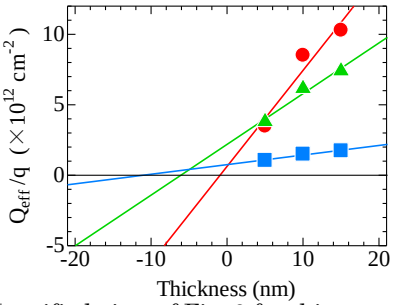

Fig.3 Magnified view of Fig. 2 for thin samples (5-15nm)

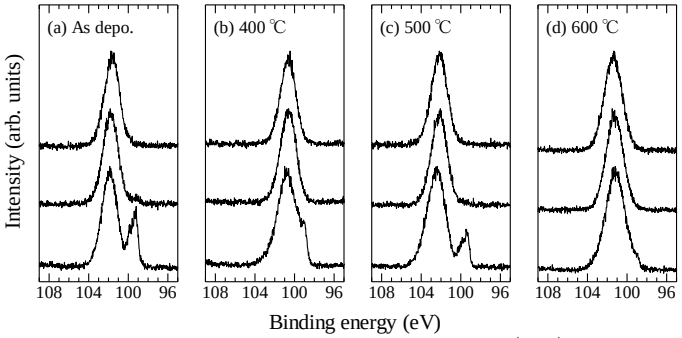

Fig.4 Si 2p core-level spectra of Sr_2SiO_4/p-Si(100) samples (a) without annealing, and annealed at (b)400°C, and (c)500°C, and (d)600°C.