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Quantitative study of interfacial properties in monolayer MoS_2 FET

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Abstract

Interfacial properties of exfoliated monolayer MoS_2 are systematically studied by both *C-V* and *I-V* with the help of 10-nm Al_2O_3 top gate oxide FET structure. The equivalent circuit analysis allows to extract interface states density (D_{it}) to be ~10^{12} $cm^{-2}eV^{-1}$, which is consistent with that obtained by *I-V*. D_{it} band tail exists close to conduction band.

1. Introduction

MoS_2 have attracted much attention in ultimate scaled device research due to its natural thin body (0.65 nm per layer) without dangling bonds [1,2]. However, both defects such as sulfur vacancy in MoS_2 and dangling bonds from gate oxide could severely degrade its interface, which has been characterized by electrical measurements, scanning transmission electron microscopy and so on [3-5]. The estimation of interface states density (D_{it}) based on subthreshold swing (S.S.) of current-voltage (*I-V*) curve is largely scattered, ranging from 10^{11}~10^{13} $cm^{-2}eV^{-1}$. While capacitance - voltage (*C-V*) measurement is known as one of effective methods to study interfacial properties quantitatively thanks to the frequency response. Both MOSCAP and MOSFET structure have been studied for *C-V* measurement of MoS_2 interface properties. In case of MOSCAP structure, relatively low D_{it} (10^{11}~10^{12} $cm^{-2}eV^{-1}$) is extracted for thin MoS_2 by applying high-low frequency method [6,7]. However, it often underestimates D_{it} due to the limitation of excitation frequency range. It is shown that D_{it} peak exists close to conduction band for thick MoS_2 by Terman method [8]. While for MOSFET structure, CVD monolayer MoS_2 is reported to have large D_{it} over 10^{13} $cm^{-2}eV^{-1}$ [3]. It is still controversial that the large frequency dispersion of *C-V* curve comes from whether series resistance or poor interface properties. In this paper, FET structure is selected to systematically compare both *C-V* and *I-V* measurements and the interface properties are evaluated for relatively high quality monolayer mechanically-exfoliated MoS_2.

2. Experiments

Monolayer MoS_2 films are mechanically exfoliated on SiO_2 (90 nm)/n^+-Si substrate from natural bulk MoS_2 flakes. Ni/Au was deposited as source/drain electrodes. Then, 1-nm Y metal was deposited via thermal evaporation of the Y metal in a PBN crucible at an Ar atmosphere with a partial pressure of 10^{-1} Pa, followed by oxidization at atmosphere to form buffer layer. 10-nm Al_2O_3 oxide layer was deposited by atomic layer deposition. The Raman measurement was employed for determining the layer number. The electrical measurements were performed in the vacuum prober.

3. D_{it} estimation from S.S. in *I-V*

Fig. 1 shows the schematic drawing and the optical image of dual-gate monolayer MoS_2 FET. Films with large area (>50 μm^2) were selected for device fabrication and characterization. The typical transfer characteristics for different V_{BG} show the clear current on/off ratio of > 10^5. The trace of threshold voltage (V_{TH}) observed for the V_{TG} sweep at different V_{BG} is plotted in **Fig. 2(a)**. The V_{TH} position is controlled by the relative ratio of capacitive coupling between the top and back gates with MoS_2 channel. Therefore, the slope in **Fig. 2(b)** corresponds to $-C_{BG}/C_{TG}$. Since C_{BG} is 0.038 μF/cm^2 for the 90-nm SiO_2 with k_{SiO2} = 3.9, C_{TG} can be estimated to be 0.46 μF/cm^2. With the help of C_{TG} value, the two-probe field effect mobilities for sample 1, 2 and 3 in **Fig. 2(c)** are estimated to be 9.5, 6.0 and 2.5 $cm^2V^{-1}s^{-1}$, respectively. Although the mobility is largely underestimated due to the access region and the contact resistance, the difference in mobilities still indicates the interfacial property difference of these three samples. Indeed, highest mobility sample (sample 1) has sharpest subthreshold region, in other words, smallest S.S., as shown in **Fig. 2(c)**.

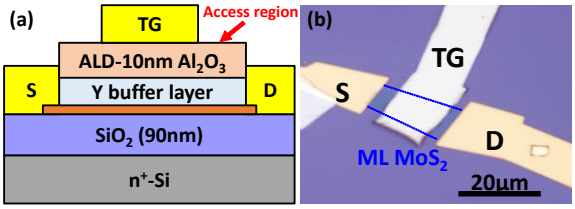

Fig. 1 (a) Schematic and (b) Optical image of dual-gate monolayer MoS_2 FET.

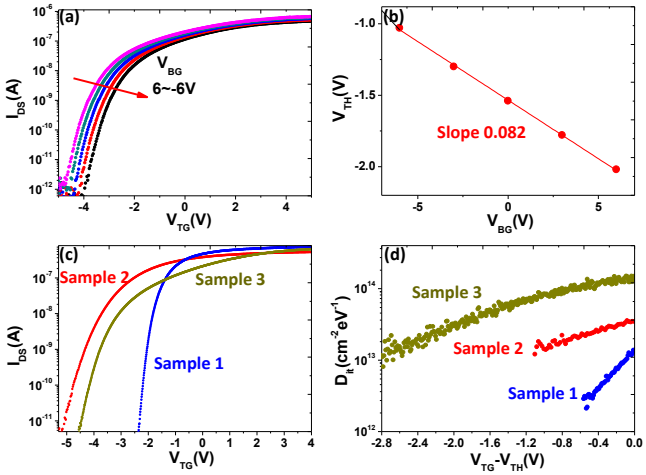

Fig. 2 (a) I_{DS}–V_{TG} characteristic for MoS_2 FET at V_{DS} = 0.1V as a function of V_{BG}. (b) Trace of the V_{TH} observed for the V_{TG} sweep at different V_{BG}. (c) Subthreshold transport characteristics of three different MoS_2 FET (V_{DS} = 0.1 V). (d) D_{it} distribution as a function of V_{TG}-V_{TH} of three samples extracted from S.S.

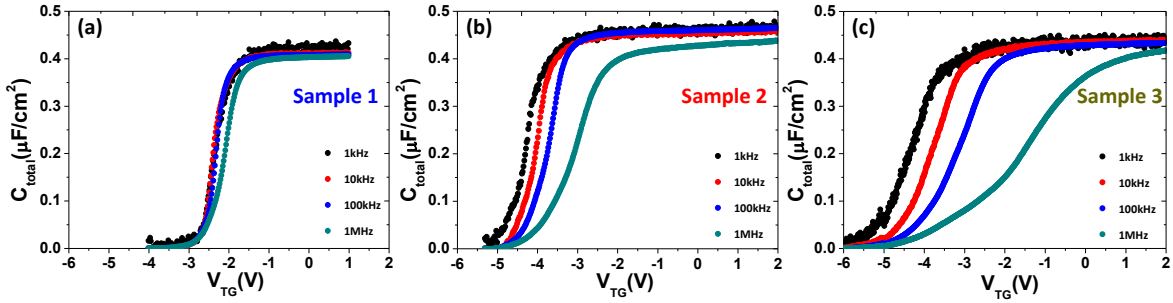

Fig. 3 *C-V* curves with frequency ranging from 1kHz -1MHz of (a) sample 1 (b) sample 2 (c) sample 3. The frequency dispersion of *C-V* is related with device performance by *I-V*. Sample 1 with high mobility and low D_{it} shows small frequency dispersion of *C-V*.

In order to study the interfacial properties quantitatively, D_{it} is extracted based on S.S. [5]. **Fig. 2(d)** shows extracted D_{it} as a function of V_{TG}-V_{TH} at subthreshold region. The highest mobility sample has lowest D_{it} level with small V_{TG} range.

3. D_{it} extraction from equivalent circuit for *C-V*

The interfacial properties are studied by using capacitance measurement for these three samples. Parasitic capacitance is carefully considered and removed. Based on the split *C-V* method, C_{total} should be zero at off-state and close to C_{ox} at on-state. So, all the *C-V* curves at different frequencies are normalized to start from zero at off-state. This procedure is reasonable because C_{ox} obtained at on-state after the normalization is consistent with C_{ox} estimated from *I-V* in **Fig. 2(b)** within the 10% error. **Fig. 3** shows C_{total}-V_{TG} curves with frequency range of 1 kHz - 1 MHz. The frequency dispersion is observed of three samples. Specifically, the sample with high mobility and low D_{it} has small frequency dispersion while the sample with low mobility and high D_{it} has large frequency dispersion. It should be mentioned that these three samples show ohmic contacts which indicates that the frequency dispersion reflects interfacial properties instead of series resistance.

In order to quantitatively study D_{it}, equivalent circuit is modelled as shown in **Fig. 4(a)**. C_{total} can be calculated based eq. (1).

$$\frac{1}{C_{total}} = \frac{1}{C_{ox}} + \frac{1}{C_Q + e^2 D_{itA}(2\pi f \tau_{itA})^{-1} \arctan(2\pi f \tau_{itA}) + e^2 D_{itB}(2\pi f \tau_{itB})^{-1} \arctan(2\pi f \tau_{itB})} \quad (1)$$

where C_{ox} and C_Q are oxide capacitance and quantum capacitance, τ_{it} is the time constant for D_{it}. By measuring capacitance as a function of frequency at fixed V_{TG}, D_{it} is estimated as shown in **Fig. 4(b)**. Although two types of interface states are considered in this equation, D_{it} are mainly come from one type of interface states and another type of interface states is not discussed here.

D_{it} from *C-V* and *I-V* have comparable range as shown in **Fig. 4(c)**, which indicates that we successfully evaluate interfacial property by electrical measurement. The lowest D_{it} obtained is ~8×10^{11} $cm^{-2}eV^{-1}$, which is one order lower than that for the previous CVD MoS_2 FET. It is expected that this improved interfacial property come from better crystallinity of mechanically exfoliated MoS_2 than CVD MoS_2. The D_{it} band tail close to conduction band is still observed for all the samples, which severely degrade device performance. By further improving MoS_2 crystallinity, this D_{it} band tail is expected to be reduced further.

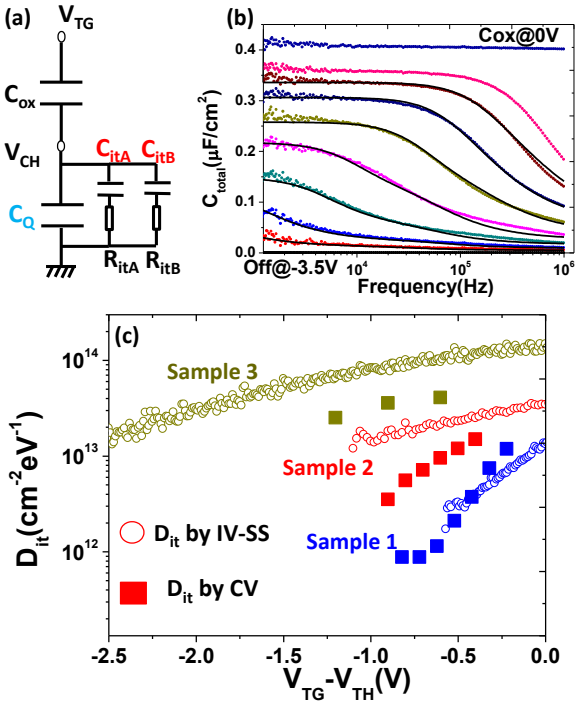

Fig. 4 (a) The equivalent circuit model of the device. (b) Capacitance as a function of frequency at fixed V_{TG} (-3.0~-2.2V with step 0.1V). Circle is experimental result and black line is fitting by eq. (1). (c) Interface states density of different samples extracted by both *C-V* and *I-V*. The extracted D_{it} are comparable by these two methods.

4. Conclusions

The interfacial properties of exfoliated monolayer MoS_2 are systematically evaluated by both *C-V* and *I-V* characterization. The D_{it} was extracted to be ~10^{12} $cm^{-2}eV^{-1}$. The D_{it} band tail close to conduction band was confirmed.

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