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Demonstration of p-type graphene barristor using a Schottky contact between graphene and p-type organic semiconductor

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Abstract

For the first time, p-type graphene barristor has been demonstrated using a Schottky contact between graphene and Dinaphtho-[2,3-b:20,30f]thieno[3,2-b] thiophene (DNTT). The drain current was successfully modulated by modulating the Fermi level of graphene in contact with the DNTT. The range of Schottky barrier height modulation was ~100meV and high on/off ratio of 10^3 has been achieved. This result compliments the n-type graphene barristor using graphene-ZnO Schottky contact and provides an essential tool for graphene barristor based complimentary circuit.

1. Introduction

Graphene barristor utilizes a Schottky contact between a graphene and a semiconductor to solve the low on-off ratio problem of graphene FET [1]. The on-off ratio of barristor is modulated by controlling the Schottky barrier height at the graphene-semiconductor interface. The Fermi level of graphene can be shifted upward or downward via an external electric field. While the first demonstration of graphene barristor used a graphene-silicon interface, following works utilized various semiconductor materials that can be deposited on a graphene because the quality of the interface between a graphene and a silicon was very difficult to manage consistently.

In order to fabricate CMOS logic circuit using graphene barristors, both n-type and p-type semiconductor should be deposited on a graphene. N-type ZnO has been investigated as a leading semiconductor candidate for n-type graphene barristor and very high on-off ratio with a reasonable drive current has been demonstrated [2]. However, p-type graphene barristor has not been demonstrated yet using a top down process compatible p-type semiconductor [3].

In this paper, for the first time, we demonstrated a p-type graphene barristor with an air-stable organic semiconductor material, Dinaphtho-[2,3-:20,30f]thieno[3,2-b]thiophene (DNTT) [4]. The on-off ratio was ~ 10^3 with a mild Schottky barrier height modulation ~ 100 meV.

2. Experiments

Fig. 1(a) shows the schematic of fabrication processes. First, the CVD graphene was transferred to SiO_2 (90nm)/ Si substrates with a vacuum transfer process and patterned with O_2 plasma using a thin Au hardmask [5, 6].

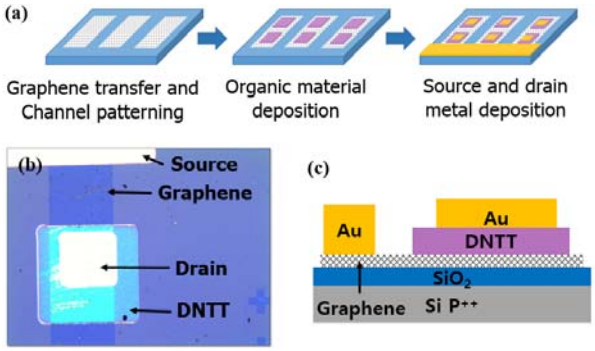

Fig. 1 (a) Fabrication process of graphene-DNTT barristor (b) Optical image of graphene-DNTT barristor, (c) Schematic vertical cross section of graphene-DNTT barristor.

Then, ~150nm DNTT was deposited using a thermal evaporator at a rate of 0.2Å/sec. A shadow mask was used to selectively deposit the DNTT only on graphene channel region. Finally, 30nm Au contact for drain was deposited using a thermal evaporator and a shadow mask process. Top down photograph of completed device is shown in Fig. 1(b). Also, a Schematic cross section of graphene-DNTT barristor is shown in Fig. 1(c).

The electric characterization was performed using a semiconductor parameter analyzer (Keithley 4200-SCS) and the Schottky barrier was extracted by measuring the temperature dependence of drain current.

3. Result and discussion

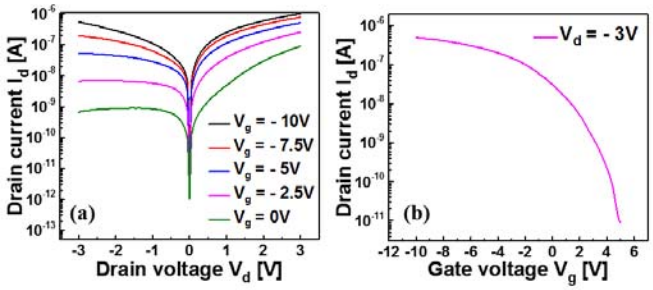

Fig. 2 (a) Output characteristics and (b) transfer characteristics of graphene-DNTT barristor

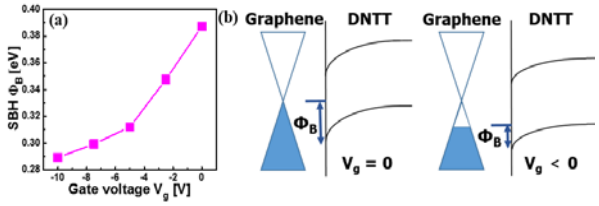

Fig. 3 (a) Schottky barrier height in relation to gate bias (b) Schematic of Schottky contact between graphene and DNTT

The output and transfer characteristics of graphene-DNTT barristor is shown in Fig.2. I_{on}/I_{off} ratio was ~ 10^3 and the drive current was ~10^{-7}A. Note that the drive current of barristor is not normalized against the channel width because the drive current is proportional to the barrier height and the graphene-DNTT contact area. The contact area of our device is roughly 10,000μm^2.

Likewise, the definition of swing is not clear for the graphene barristor because the conduction of barrister does not use a surface inversion channel. Yet, if we borrow the definition of swing defined for silicon MOSFET, the lowest swing is 600mV/dec with 90nm gate oxide for back gate control.

Another key check point for the functionality of graphene barristor is the range of Schottky barrier height modulation. To measure the Schottky barrier height, the drain current was measured at different temperatures (-50, -15, 0, 20, 40℃). The Schottky barrier height was extracted using the following diode equation.

$$I = AA^*T^2 exp(\frac{-q\varphi_b}{k_BT})[\exp\left(\frac{qV_{bias}}{\eta_{id}k_BT}\right) - 1] \quad (1)$$

where A^* is the Richardson constant which can be extracted by the diode equation. Fig. 3 (a) shows the Schottky barrier height as a function of gate voltage. The Schottky barrier height represents the difference between the Fermi level of graphene to the HOMO level of DNTT because the Fermi level of DNTT is placed near HOMO level. As schematically shown in Fig. 3(b), the Schottky barrier height is reduced when a negative gate bias increased. While 10V of back gate bias is applied through 90nm gate oxide, the range of Schottky barrier height modulation was ~100meV. While this range appears to be small, it is enough to generate 10^3 of on-off ratio because the drain current is exponentially proportional to the barrier height,

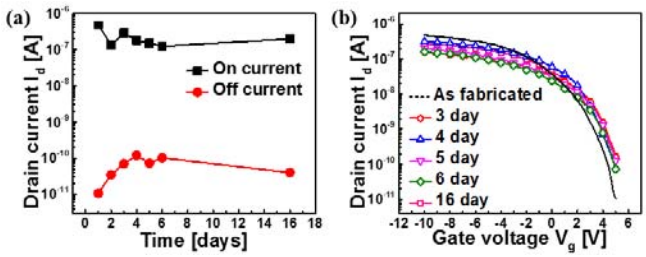

Fig. 4 (a) Time dependent on/off current and (b) Time dependent transfer characteristics of graphene-DNTT barristor.

Finally, we checked the stability of our device at room temperature by exposing the devices in air ambient because many of organic semiconductors are not stable in air ambient. As shown in Fig. 4(a), both on-current and off current were reasonably maintained for 16 days of air exposure even without a capping layer. This result can be more clearly seen by the transfer curves measured for 16 days. The transfer characteristics of graphene-DNTT barristor appear to be well maintain after the extended air exposure. This result is very encouraging because this is the first demonstration of p-type graphene barristor using a top-down process compatible material. This device can be combined with graphene-ZnO barristor and used to form a complimentary circuits.

3. Conclusions

P-type graphene-DNTT barristor has been successfully demonstrated using an organic semiconductor, DNTT. Excellent on-off ratio ~10^3 with a reasonable performance provide a very promising opportunity to form a graphene barristor based complimentary circuit. Also, very low temperature process used in this work makes graphene-DNTT barristor a good candidate for TFT applications.

Acknowledgements

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