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InAs Nanotube FETs with Atomic-Layer-Deposited Al_2O_3/ZnO Gate-Stack

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Abstract

Field-effect transistors (FETs) are fabricated using InAs/InP core-shell nanowires (NWs) with atomic-layer-deposited Al_2O_3/ZnO gate-stack. The core was selectively etched away in order to prepare a tubular InAs channel. Atomic-layer-deposition (ALD) was employed to realize axial core-gating in addition to conventional shell-gating, i.e. gate-all-around (GAA) geometry. On/Off ratio in excess of 10^5 was observed, which is larger than that in our previous GAA InAs NW-FETs, suggesting an advantage of the present scheme.

1. Introduction

Self-assembled semiconductor nanowires (NWs) grown by the vapor-liquid-solid (VLS) method are the subject of intense study nowadays due to their potential application to the future electronic and photonic devices. In particular, InAs NWs have been considered as promising candidates for n-channel materials for post-Si low-power CMOS logic applications due to their high intrinsic electron mobility. Superior FET performance is expected by introducing gate-all-around (GAA) geometry, where the channel is completely surrounded by the gate, through the enhanced electrostatic control over the channel. However, short-channel effects begin to deteriorate off-state properties even for the GAA NW-FETs when the gate length is aggressively scaled to sub-100 nm regime.

In this work, we report on fabrication of InAs nanotube FETs with an atomic-layer-deposited Al_2O_3/ZnO gate-stack, and their DC electrical characteristics. Since one can deposit a film on the inside of a tubular object by using ALD technique, it is expected that our FET has a gate that acts on both inside and outside of the tubular channel. An implementation of such core-shell dual-gating was theoretically demonstrated to exhibit better sub-threshold swing (SS) and on-current than those in the conventional GAA geometry, leading to enhanced On/Off ratio [1,2]. Our prototypical InAs nanotube FET device features On/Off ratio in excess of 10^5 whereas that in our previous GAA InAs NW-FETs was typically 10^4 or less [3,4], suggesting an advantage of the present gating scheme.

2. Experimental method and results

The NWs were grown via the Au-catalyzed VLS mode, with InP/InAs shells grown by vapor phase epitaxy in a MOVPE system. The NWs were transferred onto a Si/SiO_2 device substrate that is prepatterned with alignment marks and Ti/Au source/drain leads by using the ink-jet machine and the home-made manipulator, such that the NWs are suspended between the two Ti/Au lead lines. The source and drain regions were defined by electron-beam lithography at the NW segments crossing the Ti/Au leads. The Ohmic contacts were made to the outer InAs shell by removing the surface oxides by Ar plasma-etching, followed by evaporation and lift-off of Ti. The nanotube channel was prepared by selectively etching the core using a mixture of citric acid and hydrogen peroxide. Here, the intermediate InP shell serves as an etch-stop layer. Figure 1 shows an SEM image of the InAs nanotube with source/drain leads fabricated in this manner.

Next, the nanotube was conformally coated with 6 nm of Al_2O_3, as a gate insulator, and 20 nm of ZnO in sequence via ALD. We doped 5 % of Al to the ZnO layer to decrease the resistivity (a few mΩ･cm). Figure 2(a) and 2(b) schematically show the device structure before and after the ALD process, respectively. Because of the conformal nature of ALD, the Al_2O_3/ZnO gate-stack is formed not only on the outside of the nanotube as GAA and gate-overlap structure, but also on the inside of the nanotube, implementing the core-shell dual-gate geometry.

DC electrical characterization of the FET was performed at room temperature with a semiconductor parameter analyzer (Agilent B1500A). Figure 3 shows transfer characteristics of the fabricated device, in which the outer diameter of the InAs tube is 120 nm and the gate length, L_g, is 200 nm. The outer and inner gates are not separated, and are biased with the same gate voltage. The obtained On/Off ratio is in excess of 10^5, which is larger than that in our previous GAA InAs NW-FETs [3,4] by more than one order of magnitude. The improved FET performance suggests an advantage of the core-shell dual gating scheme.

3. Conclusions

We have fabricated InAs nanotube FETs with atomic-layer-deposited Al_2O_3/ZnO gate-stacks. The improved FET performance demonstrates an advantage of using core-shell dual gating on a tubular channel.

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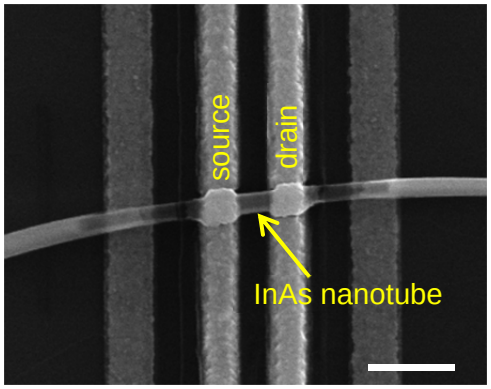

Fig. 1 SEM image of the InAs nanotube fabricated by selective etching of the InAs core. The scale bar is 500 nm.

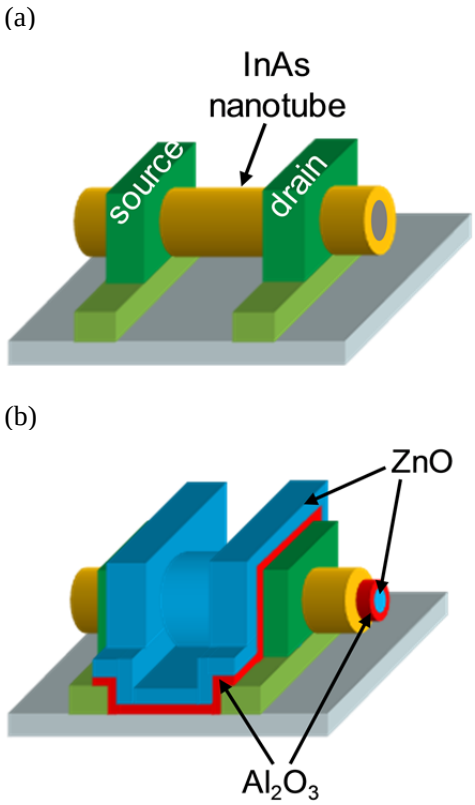

Fig. 2 Schematic device structure of the nanotube FET (a) before and (b) after ALD of Al_2O_3/ZnO gate-stack.

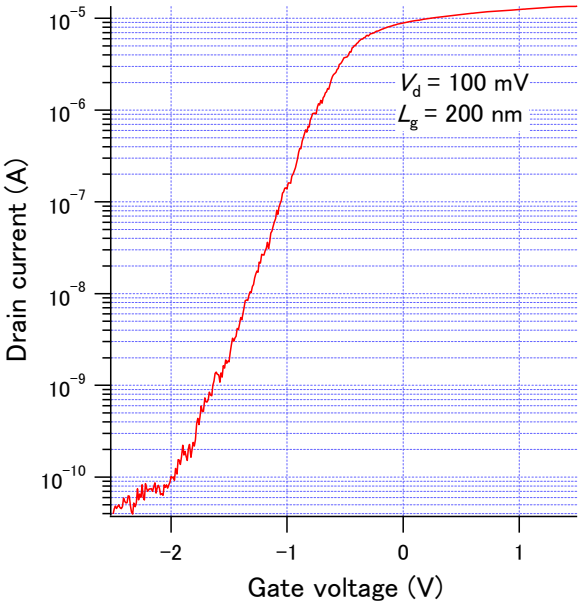

Fig. 3 Drain current – gate voltage characteristics of the fabricated device for V_d = 100 mV.