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Characterization of near-interface border-traps in GeO_2/Ge gate stacks grown by low and high temperature thermal oxidation using deep-level transient spectroscopy

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Abstract

We developed a method for characterizing the near-interface border-traps (BTs) in GeO_2/Ge gate stacks using deep-level transient spectroscopy. The BT density (N_{BT}) in p-MOS grown by low temperature oxidation is smaller than that by high temperature oxidation. By contrast, the N_{BT} in n-MOS is almost the same regardless of the oxidation temperature. In addition, the N_{BT} in p-MOS is drastically decreased by Al post metallization annealing (Al-PMA), but the N_{BT} in n-MOS is not decreased. These results suggest that the species of BT in n-MOS are different from that of p-MOS.

1. Introduction

To fabricate high-performance Ge MOSFETs, a high-quality gate-stack formation on Ge is essential. However, border-traps (BTs) near the GeO_2/Ge interface are still a serious issue that degrades the performance of Ge MOSFETs, although a GeO_2/Ge structure is beneficial to a decrease in interface-traps (ITs). This is the reason why the BT characterization is important to realize high-performance Ge MOSFETs. In this study, we prepared two kinds of MOS capacitors (CAPs) with a structure of SiO_2/GeO_2/Ge. One was a relatively thick GeO_2 by thermal oxidation at 550°C, at which GeO volatilization should be occurred at the GeO_2/Ge interface. Another was thin GeO_2 by the oxidation at 425°C, at which the volatilization should not be occurred. We investigated BTs in these MOSCAPs using deep-level transient spectroscopy (DLTS) method. The Al post metallization annealing (PMA) effect on BT passivation was also studied.

2. Experimental

Both p- and n-type (100) Ge substrates with respective doping concentrations of 2.3×10^{16} and 9.3×10^{15} cm^{-3} were used. After substrate cleaning, SiO_2/GeO_2 bilayer passivation was performed [1]. Here, the thicknesses of SiO_2 and GeO_2 layers were ~1 nm each. Next, post thermal oxidation (PTO) was performed at 550°C for 15 min or 425°C for 9 h in O_2 ambient. After 14-nm-thick SiO_2 was deposited on the both samples, the annealing at 400°C for 30 min in N_2 was performed. Then, the Al gate film was deposited on the SiO_2 surface by thermal evaporation. Before the electrode patterning, an optional PMA was carried out at 300°C for 30 min in N_2, which is the Al-PMA. Finally, electrode patterning and back-contact formation by In-Ga alloy were performed. A schematic diagram of sample structure is shown in Fig. 1 (a). The equivalent oxide thicknesses (EOTs) of the MOSCAPs with PTO at 550 and 425°C were ~19.5 and 16.8 nm, corresponding to GeO_2 thicknesses of 6.6 and 2.6 nm, respectively.

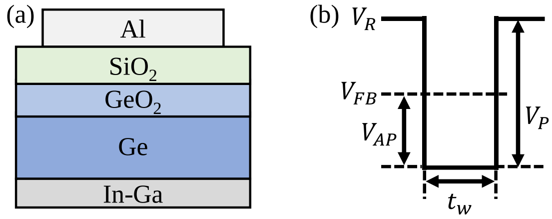

Fig. 1 (a) sample structure and (b) pulse sequence for DLTS measurement.

DLTS measurements were performed using a lock-in integrator. The rectangular injection pulse is shown in Fig. 1(b). V_R is the quiescent reverse-bias voltage, which was set at a value corresponding to band bending of ϕ_B (ϕ_B is the energy difference between Fermi-level and intrinsic Fermi-level) [2]. V_P is the pulse height from V_R, and V_{FB} the flat band voltage. V_{AP} ($=|V_P-V_{FB}|$) is the accumulation pulse voltage, which is an important parameter for the BT analysis, because the injection pulse intensity (E_{AP}) at the GeO_2/Ge interface is given by $E_{AP}=V_{AP}$/EOT. Frequency (f) and pulse width (t_w) are also important parameters for selecting the observed BT position (z_0) and for filling with carriers into BTs, respectively. In this work, f=10 Hz were used, which corresponds to z_0=1.4 nm from the interface for p-MOS and z_0=2.0 nm for n-MOS.

3. Results and discussion

Figure 2 shows DLTS signal intensity (I_{DLTS}) dependence on V_P with a maximum t_w of 5 ms at different temperatures (Ts) for a MOSCAP with PTO at 550°C and without Al-PMA. Here, $\Delta C/C(\infty)^3$ is plotted as I_{DLTS} because both BT density (N_{bt}) and IT density (D_{it}) are proportional to $\Delta C/C(\infty)^3$ (ΔC is the DLTS raw signal and $C(\infty)$ is the capacitance at equilibrium). Let us pick up the result at 80 K as an example. The I_{DLTS} drastically increased when the V_P increased from 0 to 0.5 V. Note 0.5 V is approximately the V_{FB} at 80 K for this sample. Therefore, this increase is dominated by the capture process of IT [2]. We believe that the weakest injection condition (t_w=2 μs) under E_{AP}=0 MV/cm is enough to compose the IT signals. Therefore, we use these data for D_{it} calculation. In the case of V_P > 0.5 V, namely accumulation was established, the contribution of IT would be saturated due to the completion of IT capture. As the result, the increase in I_{DLTS} with V_P > 0.5 V was governed by the capture process of BT because of an increase in hole numbers at Ge side of the GeO_2/Ge interface. After subtracting the IT signal from I_{DLTS}, we calculate the N_{bt}, details of which will be presented in the conference.

Figures 3 (a) and 3(b) represent energy distributions of D_{it}s for MOSCAPs with PTO at 550 and 425°C, respectively. It was confirmed that D_{it} values are almost identical despite the PTO temperature difference, implying that the interface properties is not influenced by GeO volatilization. The Al-PMA is effective for a decrease in D_{it} near the valence band edge but is not near the conduction band edge (rather worsen), which are consistent with our previous conclusion [2, 3].

Figures 4 (a) and 4(b) represent dependence of N_{bt} on T for p-MOSCAPs with PTO at 550 and 425°C, respectively; Figures 5 (a) and 5(b) represent the similar results for n-MOSCAPs with PTO at 550 and 425°C, respectively. It was confirmed from these results that 1) the N_{bt} for p-MOS with 425°C-PTO is a half of that with 550°C-PTO under E_{AP}=2 MV/cm, suggesting BT in p-MOS is associated with GeO volatilization; 2) the N_{bt} for p-MOS is drastically decreased by Al-PMA; 3) the N_{bt}s for n-MOS with PTO at 425 and 550°C are almost the same and is not decreased by Al-PMA, suggesting the species of BT in n-MOS are different from that of p-MOS.

4. Conclusions

Near-interface BT in GeO_2/Ge structures were characterized by DLTS. The N_{bt} in p-MOS were drastically decreased by Al-PMA, but the N_{bt} in n-MOS was not decreased. This is a reason for difficulty of the electron mobility enhancement.

Acknowledgements

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References

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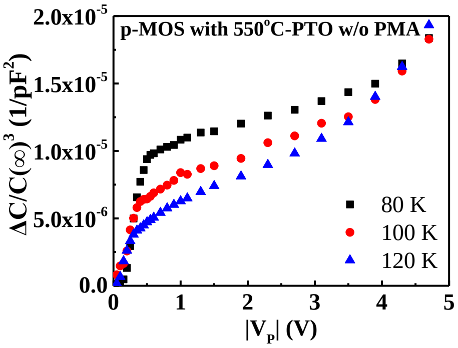

Fig. 2 I_{DLTS} dependence on V_P for a p-MOS with PTO at 550°C without Al-PMA.

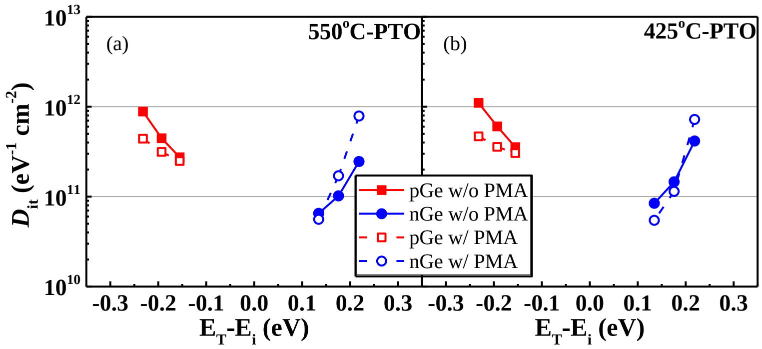

Fig. 3 Energy distributions of D_{it}s for MOSCAPs with (a) 550°C-PTO and (b) 425°C-PTO. The results for MOSCAPs with Al-PMA are also shown.

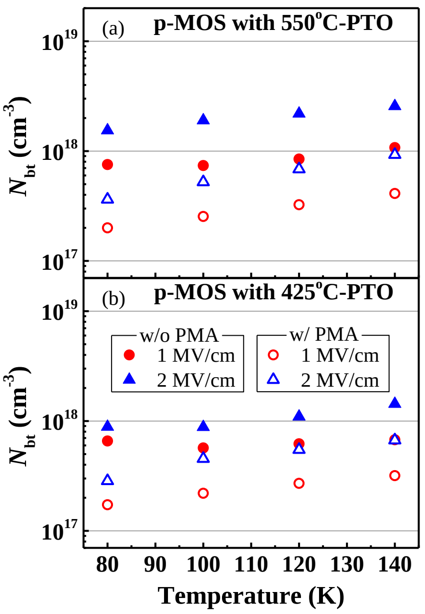

Fig. 4 Dependence of N_{bt} on T for p-MOS with (a) 550°C-PTO and (b) 425°C-PTO. The results with Al-PMA are also shown.

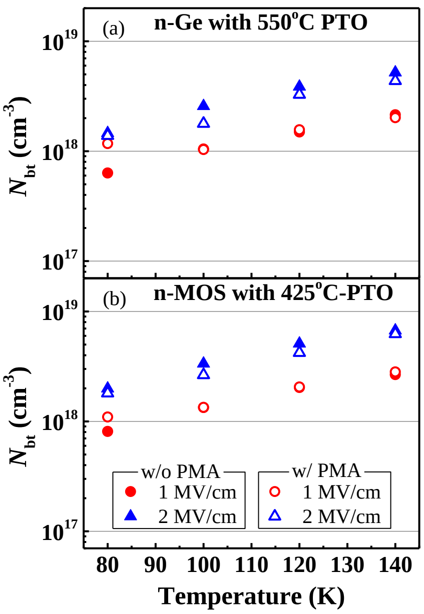

Fig. 5 Dependence of N_{bt} on T for n-MOS with (a) 550°C-PTO and (b) 425°C-PTO. The results with Al-PMA are also shown.