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A 190mV Start-up Voltage Doubler Charge Pump with CMOS Gate Boosting Technique in 0.18μm Standard CMOS Process for Energy Harvesting

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Abstract

A charge pump circuit that can start-up from 190mV is proposed and demonstrated. The proposed circuit uses inverter level shifter to generate sufficient gate voltage swing to both main NMOS and PMOS power transistors to enhance the channel conductance. The proposed circuit is implemented by a standard 0.18μm CMOS process and the measurement result shows that output power increases by 181% compared with the conventional forward-body-bias scheme.

1. Introduction

Energy harvesting is expected to be another main power source to charge the battery or to drive small devices without battery in IoT solutions. The power management circuit needs to start-up by itself (cold start) with the output voltage of the harvester [1]. Typically, output voltage is below 200mV for a thermal energy harvester and around 200 ~ 500mV for a photovoltaic cell in the indoor light condition. Thus, the start-up circuit has to cover these voltage ranges of V_{IN}. Moreover, such a low input voltage requires sub-threshold voltage circuit operation.

Recently, many start-up charge pumps are reported based on the CMOS voltage doubler as shown in Fig. 1 for its low voltage operation capability [2-6]. The channel resistance R_{on} of the power transistors directly affects the circuit efficiency. To decrease R_{on}, a forward-body-bias (FBB) voltage doubler charge pump circuit has been reported in [3] as shown in Fig. 2. However, circuit efficiency becomes worse when V_{IN} exceeds around 300mV due to the FBB diode leakage. PMOS gate voltage boosting schemes are proposed to decrease the main PMOS R_{on} in [4-6] as shown in Fig. 3. However, gate boosting for the main NMOS transistor has still not been realized in the start-up charge pump. In this paper, a new voltage double to reduce R_{on} of both NMOS and PMOS power transistors (CMOS gate boosting) is proposed and realized.

2. Proposed Charge Pump Circuit

Architecture block diagram of the proposed circuit is shown in Fig. 4. The proposed circuit consists of ring oscillator, clock driver, 2-stage charge pump cells, NMOS boosting level shifter (NBLS), PMOS boosting level shifter (PBLS), and auxiliary pump (AUX pump) support the main pump operation in each stage. Fig. 5 is the operation waveforms of NBLS / PBLS and Figs. 6(a) and 6(b) show the circuit detail schematics of Stage-1 and Stage-2, respectively. NBLS and PBLS are simple CMOS inverters. NBLS provides $2V_{IN}$ (V_{IN} is input supply voltage) swing to NBA and NBB which are connected to the gate of main NMOS power transistors via capacitor while PBLS provides $2V_{IN}$ swing to main PMOS. Therefore, R_{on} of main NMOS and PMOS power transistors is greatly reduced.

A short circuit current through the main NMOS and PMOS power transistors are avoided for efficient boosting by using non-overlapping and overlapping gate clock, respectively. A short current in NBLS and PBLS is also carefully minimized by optimizing pumping capacitors and transistor size to maintain slew rate of the clock signals.

3. Measurement Results

The proposed circuit is implemented by a 0.18μm standard CMOS technology. Conventional 2-stage FBB scheme [3] is also implemented for comparison. Fig. 7 shows a die photo of the test chip. The minimum input voltage of 190mV with an output of 480mV is obtained in the proposed scheme as shown in Fig. 8. Relatively large ripple is due to the light capacitive load of 9pF compared to 10.8pF pumping capacitance. Fig. 9 shows measured V_{OUT}-V_{IN} characteristics for an open load condition. V_{OUT} of FBB scheme degrades at V_{IN}>300mV by FBB leakage while the proposed scheme does not. Fig. 10 shows V_{OUT} and P_{OUT} as a function of I_{OUT} at V_{IN}=300mV. I_{OUT} and P_{OUT} of the proposed scheme are much higher than the conventional FBB scheme at their maximum P_{OUT}. Table I summarizes the circuit performances of the start-up charge pumps. Although the proposed scheme uses matured process, the minimum V_{IN} is below 200mV compared with others.

4. Conclusions

The proposed voltage doubler charge pump circuit for energy harvesting is demonstrated in 0.18μm standard CMOS process. R_{on} of the main power transistors is significantly decreased by gate boosting. The measured minimum V_{IN} for start-up operation is 190mV. 146% and 181% improvement of the I_{OUT} and P_{OUT} are achieved from the conventional FBB scheme, respectively.

Acknowledgements

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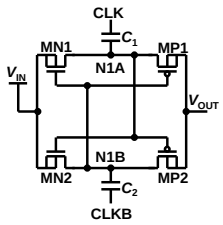

Fig. 1 Conventional voltage doubler charge pump cell [2].

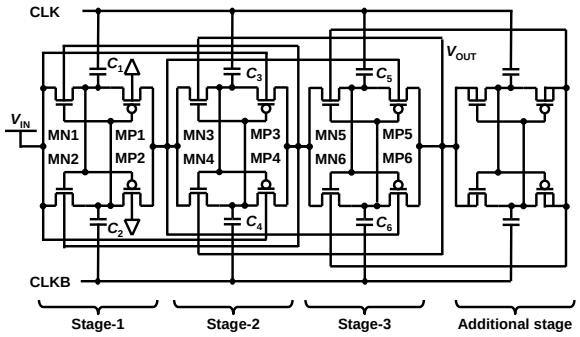

Fig. 2 2-stage FBB voltage doubler charge pump [3].

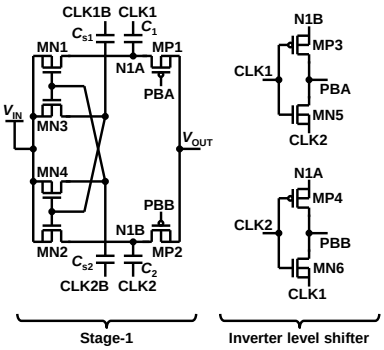

Fig. 3 Voltage doubler using inverter level shifter for PMOS gate boosting [5].

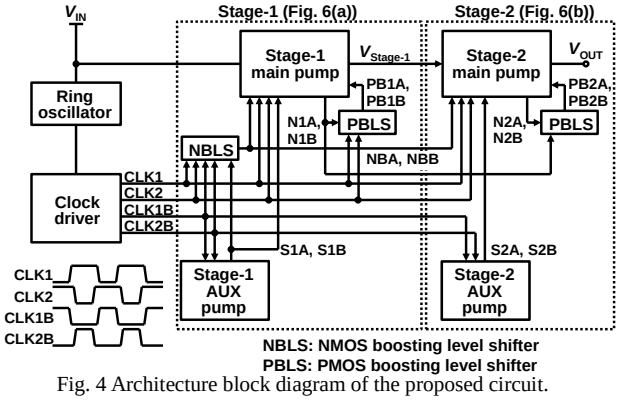

Fig. 4 Architecture block diagram of the proposed circuit.

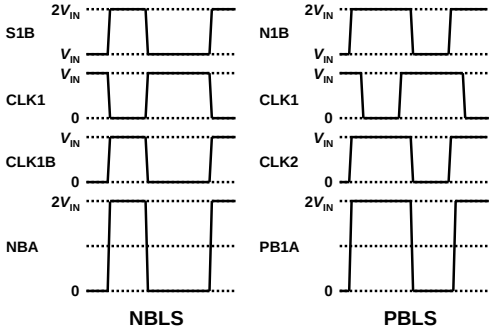

Fig. 5 Operation waveforms of the NBLS and PBLS.

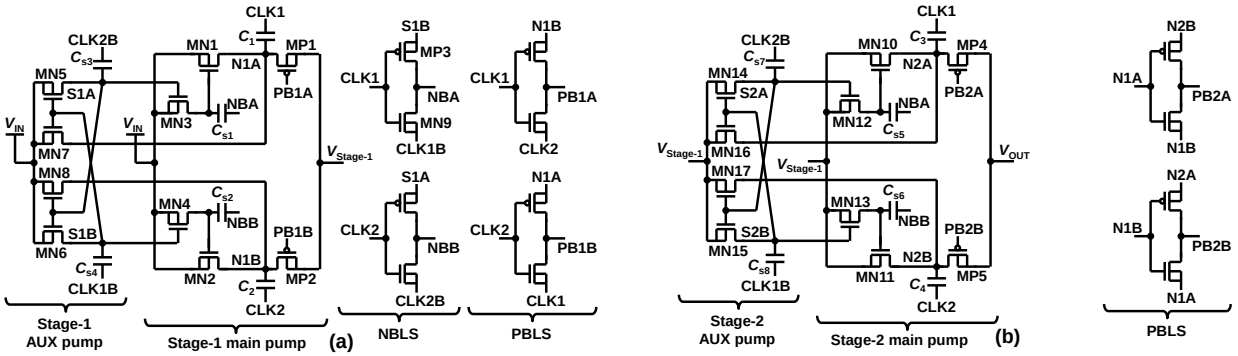

Fig. 6 Proposed boost charge pump circuit detail. (a) Stage-1 and (b) Stage-2. Main power transistors are MN1, MN2, MP1, MP2, MN10, MN11, MP4, and MP5.

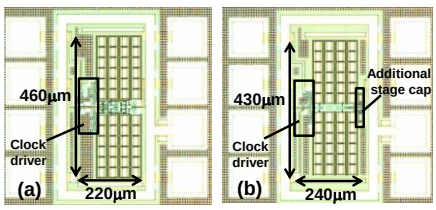

Fig. 7 Micrograph of the test chip. (a) Proposed charge pump and (b) Conventional FBB charge pump [3].

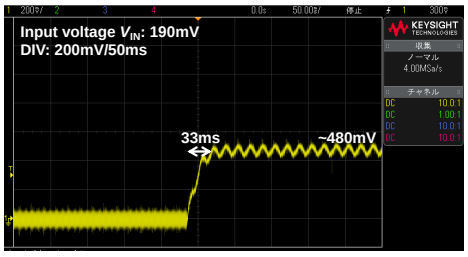

Fig. 8 Measured output waveform at V_{IN}=190mV.

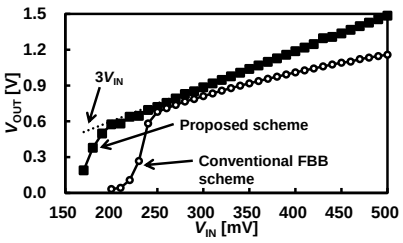

Fig. 9 Measured V_{OUT}-V_{IN} characteristics.

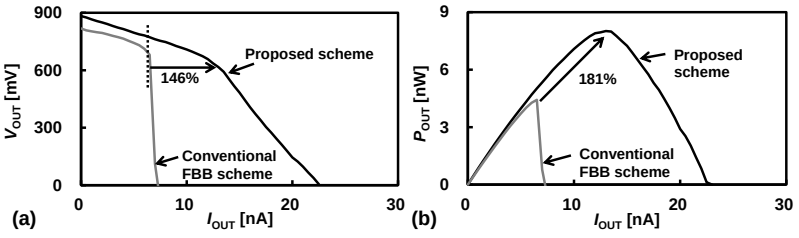

Fig. 10 Measured (a) V_{OUT} and (b) P_{OUT} as a function of I_{OUT}.

Table I Performance summary and comparison.

Ref.	[3]	[4]	[5]	This work
Process (nm)	65	130	180	180
Scheme	FBB	PMOS enhance	PMOS enhance	CMOS enhance
No. of stages	3-stage	3-stage	2-stage	2-stage
Min. Input Voltage (V)	0.18	0.15	0.21	0.19
Output Voltage (V)	0.6 (@0.18V)	0.62 (@0.18V)	0.6 (@0.21V)	0.48 (@0.19V)
f_{Clock} (Hz)	10M	250K	6K	77K (@300mV) (simulation)
Pumping Cap (F)	12.3p	10 nF (Off-chip)	103p	10.8p