Extended Abstracts of the 2017 International Conference on Solid State Devices and Materials, Sendai, 2017, pp511-512

K-2-02

A Wide Load Range Switched Capacitor DC-DC Converter with Adaptive Bias Comparator for Ultra-Low-Power Power Management Integrated Circuit

Hiroki Asano, Tetsuya Hirose, Yuta Kojima, Nobutaka Kuroki, and Masahiro Numa

Dept. of Electrical and Electronic Engineering, Kobe University
1-1, Rokkodai, Nada, Kobe 657-8501, Japan
Phone: +81-78-803-6075, Email: {hiroki@cas., hirose@}eedept.kobe-u.ac.jp

Abstract

This paper presents a wide load range switched-capacitor (SC) DC-DC buck converter with an adaptive bias comparator for ultra-low-power power management integrated circuit (ULP-PMIC). The proposed converter is based on the conventional one and modified to be able to operate in a wide load range by using the adaptive bias comparator. Measurement results demonstrated that the proposed SC DC-DC converter generates a 1.0-V output voltage from a 3.0-V input voltage in the load range up to 100 µA. The power conversion efficiency was more than 60% in the load range from 0.8 to 100 µA.

1. Introduction

Ultra-low-power power management integrated circuits (ULP-PMICs) are strongly required for next generation IoT/IoE (internet of things/everything) applications because they have to supply appropriate voltages for circuits with a limited energy source. In this paper, we propose a fully integrated and wide load range switched-capacitor (SC) DC-DC converter for ULP-PMIC.

An SC DC-DC converter has attracted much attention as a core circuit of the PMIC because it can be fully integrated on a chip [1-4]. The converter can generate a buck or boost voltage by connecting capacitors in series or parallel with dedicated control signals. Therefore, the control circuits must be designed with ultra-low power dissipation to achieve higher power conversion efficiency. Kojima *et al.* proposes a high-efficiency SC DC-DC converter with fully on-chip configuration [3]. The converter employs pulse frequency modulation (PFM) control, whose operation frequency changes according to the load current, to achieve ultra-low power dissipation of the control circuit [3]. However, the load range is limited to less than several micro ampere (< a few µA). This is because the clock frequency of the PFM control circuit increases when the load current increases, and thus the low-power comparator used in the converter is not able to operate at higher frequency.

To solve the problem, we develop a wide load range SC DC-DC converter using an adaptive bias comparator. The converter is based on the conventional one [3] and modified to be able to operate in a wide load range by using the adaptive bias comparator. Because the bias current of the comparator increases as the load current increases, the proposed converter can operate in a wider load range.

2. Proposed circuit

Figure 1 shows a block diagram of the proposed SC DC-DC buck converter. The proposed circuit consists of a voltage and current reference circuit, start-up/fail-safe circuit, PFM control circuit, non-overlap clock generator, complementary

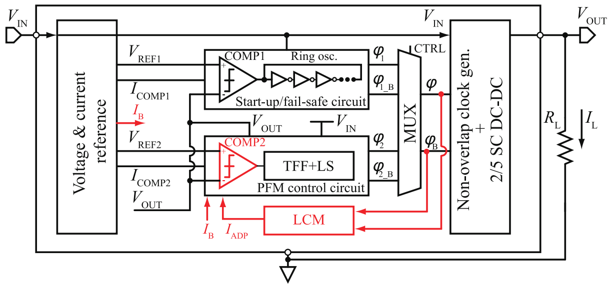

Fig. 1 Proposed SC DC-DC converter.

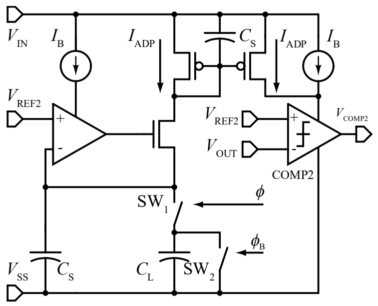

Fig. 2 Schematic of the load current monitor (LCM).

2/5 SC DC-DC converters, and load current monitor (LCM). Different from the conventional converter [3], we develop the LCM to achieve a wide load range operation. Details of the circuit operation are described as follows.

The start-up/fail-safe and PFM circuits are the control circuits for the complementary SC converters. The SC converters accept an input voltage V_{IN} and generate an output voltage V_{OUT} with the conversion ratio of two-fifth (i.e., $V_{OUT} = 2/5 \times V_{IN}$). The start-up/fail-safe circuit consists of a comparator (COMP1) and a ring oscillator. It generates a clock signal for the SC DC-DC converters at the start-up and fail conditions. The PFM control circuit consists of a comparator (COMP2), toggle flip-flop (TFF), and level shifter (LS). It generates a clock signal for the converters at the steady-state condition. To reduce power dissipation of the PFM circuit, the PFM circuit is driven by V_{OUT}, which is lower than V_{IN}. The LS converts signal level of the PFM circuit into full-swing voltage level of V_{IN}. The voltage and current reference circuit generates reference voltages (V_{REF1} and V_{REF2}) and bias current (I_B) with nano-watt power dissipation.

Figure 2 shows a schematic of the LCM and CMOP2. The LCM consists of an OPAMP, switches $SW_{1,2}$, capacitors $C_{L,S}$, and current mirror circuit. The C_L and two switches $SW_{1,2}$ driven by clock pulses ϕ, ϕ_B form a SC resistor. The resistance can be expressed as $(C_L \cdot f)^{-1}$, where C_L is the load capacitance and f is the switching frequency. Therefore, current I_{ADP} generated by the LCM is given by

$$I_{ADP} = f \cdot C_L \cdot V_{REF2}. \quad (1)$$

In the PFM control scheme, the switching frequency f increases as the load current I_L increases. Therefore, the I_L is also given by

$$I_L = f \cdot kC_L \cdot \Delta V_{Ripple}, \quad (2)$$

where k is ratio and ΔV_{Ripple} is ripple voltage. Thus, from Eqs. (1) and (2), the I_{ADP} is rewritten as

$$I_{ADP} = \alpha \cdot I_L, \quad (3)$$

where α is $V_{REF2}/k{\cdot}\Delta V_{Ripple}$. Because the bias current of the COMP2 is I_B+I_{ADP} and I_{ADP} is proportional to I_L, the proposed SC DC-DC converter can operate in a wide load range.

3. Measurement results

A prototype chip was fabricated with a 0.13-µm 1P4M CMOS process with deep n-well option. Figure 3 shows a chip micro graph and its layout (area: 1.82 mm^2). The reference voltages and bias current (V_{REF1}, V_{REF2}, and I_B), were designed to be 0.5, 1.0 V, and 1.2 nA, respectively.

Figure 4 (a) shows the measured waveforms of the proposed SC DC-DC converter at the startup condition. The V_{OUT} increased and settled to V_{REF2}. The settling time was 2 ms. Figure 4 (b) shows the measured waveform of the proposed SC DC-DC converter at the steady-state condition when I_L was 455 nA. The ripple voltage ΔV_{Ripple} was within 0.2 V.

Figure 5 shows the power conversion efficiency of the proposed and conventional circuits as a function of the load current. The load range of the proposed circuit increased 20 times higher than that of the conventional one. The efficiency was more than 60% in the load range from 0.8 to 100 µA with a 1-V output voltage. Note that, even in the range from 0.2 to 1 µA, our proposed circuit achieved more than 50% power conversion efficiency. We confirmed that the LCM enables our proposed circuit to operate in a wide load range with high efficiency. Thus, our proposed circuit is useful for ULP-IoT devices.

4. Conclusion

In this work, we developed an SC DC-DC converter with an adaptive bias comparator for ULP-PMIC. The LCM enabled the converter to operate in a wide load range with high efficiency. Measurement results demonstrated that the proposed SC DC-DC converter generates a 1.0-V output voltage from a 3.0-V input voltage in the load current range up to 100 µA. The power conversion efficiency was more than 60% in the load range of 0.8 to 100 µA.

Acknowledgements

This work was partially supported by LAPIS semiconductor Co., Ltd., VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Cadence Design Systems, Inc., Mentor Graphics, Inc., KAKENHI (JP15H01679), and the New Energy and Industrial Technology Development Organization (NEDO).

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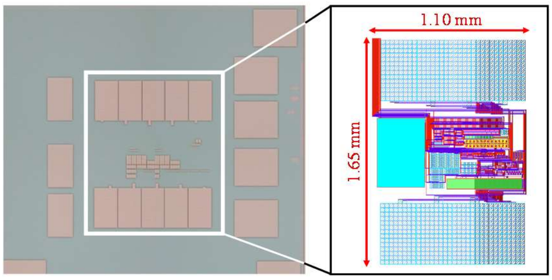
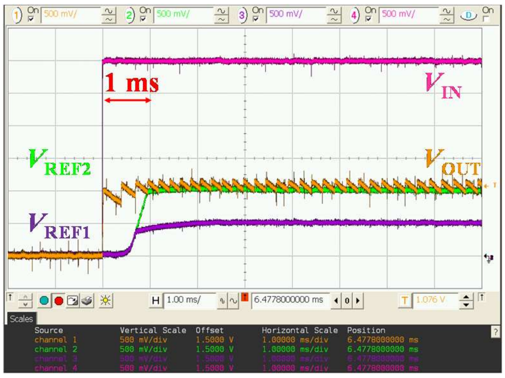
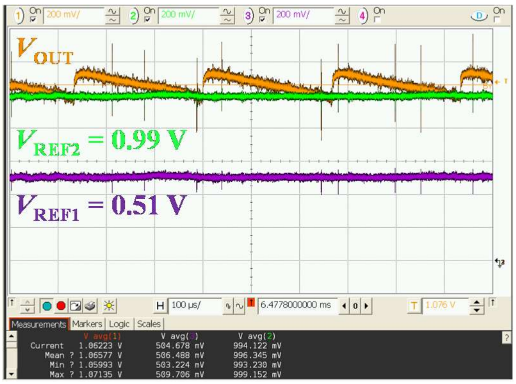


Fig. 3 Chip micrograph and layout of the proposed circuit.



(a)



(b)

Fig. 4 Measured waveforms at (a) startup and (b) steady-state.

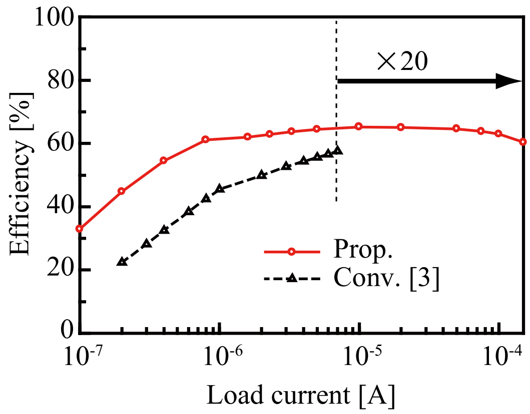


Fig.5 Power conversion efficiency as function of load current