K-2-03

Comparisons of Wire Bonding and Flip-Chip Bonding Assembly in High Frequency Hysteretic DC-DC Buck Converters

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Abstract

This paper compares high frequency hysteretic buck converters assembled by chip-on-board wire bonding and flip-chip bonding scheme in terms of efficiency, switching frequency and operation stability. Using 0.35μm standard CMOS process 5V I/O transistors, 5-30MHz operation is demonstrated with 88.5% efficiency at 2.8W output in the flip-chip bonding sample and 87.1% at 2.7W in the wire bonding. However, unstable oscillation is observed in the wire bonding scheme. Flip-chip bonding scheme is essential for efficient and stable high frequency DC-DC converter operation.

1. Introduction

Growing demands for a compact point-of-load DC-DC converter are pushing downsizing of the passive elements. In order to reduce the reactance, switching frequency f_{SW} is increased. However, in a high frequency DC-DC converter, typically above 1MHz in low voltage applications, large ringing caused by parasitic LC resonant tanks and reduced efficiency due to parasitic resistance severely harm the performance and reliability of the DC-DC converters when conventional wire bonding (WB) assembly scheme is used [1]. In addition, active area is increased by WB. Instead, flip-chip bonding (FCB) assembly is becoming widely used for its smaller active area and reduced parasitic impedance [2-4]. In this paper, WB and FCB assembly schemes are compared in high frequency hysteretic DC-DC buck converter and the superiority of FCB is quantitatively shown and discussed.

2. Circuit design and evaluation board implementation

The circuit block diagram of the hysteretic DC-DC buck converter used in this work is based on [5], as shown in Fig. 1. The switching frequency f_{SW} is determined by the time constant $R_{FB}C_{FB}$, the hysteresis window voltage V_{HYS} and the delay time of the circuits in the oscillation path. In this work, the resistance of R_{FB}, R-2R ladder (R_{HYS}), and dead time (DT) are variable by external signals to change f_{SW} during the evaluation. The circuit has been implemented in a standard 0.35μm CMOS process with 5V I/O transistors.

Chip-on-board (COB) assembly by Au WB and Au stud bump FCB scheme is used to connect the chip and evaluation board as shown in Fig. 2. Fig. 3 shows the chip micrograph of the fabricated chip. The active chip area is 1.8mm× 1.0mm. Fig. 4 shows the photograph and X-ray micrograph of the FCB COB assembly. An anisotropic conductive film (ACF) is inserted between the chip and board for FCB adhesion. A SMT NiZn ferrite core inductor L=100nH and output capacitor C_{OUT}=21μF are used (see Fig. 1).

3. Measurement Results

All measurements are conducted at V_{DD}=5V and V_{REF}= 3.7V. Output voltage V_{OUT} ranges within 3.3-3.6V according to the load conditions. The measured efficiency as a function of f_{SW} at output current I_{OUT} of 800mA is shown in Figs. 5(a) and 5(b). Higher efficiency is achieved at the shortest DT, since NMOS body diode conduction loss decreases. The buck converter shows the maximum efficiency of 87.1% at 2.7W output in the WB sample whereas 88.5% efficiency is obtained at 2.8W output in the FCB. The FCB sample shows 1.0-1.5% higher efficiency compared to the WB due to the smaller series resistance. Unstable oscillation is observed in the WB sample around f_{SW}=13-14MHz. Fig. 6 shows measured efficiency vs. I_{OUT}. The highest efficiency of 86.4% and 87.6% are observed in the WB and FCB sample, respectively. I_{OUT} dependence of f_{SW} is shown in Fig. 7 where f_{SW} is set to the highest mode. In the WB sample, unstable oscillation mode is observed at I_{OUT}=300-500mA. Figs. 8(a)-(d) show measured V_X and V_{OUT} waveforms at the highest f_{SW} setting. Fig. 8(a) shows the typical oscillation instability in the WB sample whereas such a problem is not observed in the FCB sample (Fig. 8(b)). The output voltage V_{OUT} ripple is also degraded in the WB sample as shown in Figs. 8(c) and 8(d). Figs. 9(a) and 9(b) plot measured f_{SW} vs. R_{HYS} code. The operation instability mainly appears when R_{HYS} code is set to a certain f_{SW} range.

Simulations are performed to consider the operation instability in the WB sample. The simulated V_X, V_{CMP}, V_{FB}, and V_{INP} waveforms (see also Fig. 1) are shown in Figs. 10(a) and 10(b). Large resonant oscillation and noise induced by parasitic LC tanks are observed in Fig. 10(a). Table I summarizes the differences between the COB assembly schemes.

4. Conclusions

In this paper, 0.35μm CMOS high frequency hysteretic DC-DC buck converters with COB WB and FCB assembly are compared. Measured efficiency is improved by 1.0-1.5% and the maximum efficiency of 88.5% is obtained in the FCB sample while operation instability is observed in the WB sample.

References

[1] M. Pavier et al., *APEC*, pp. 699-704, 2003.
[2] P. Hazucha, et al., *JSSC*, vol. 40, pp. 838-845, 2005.
[3] N. Sturcken, et al., *JSSC*, vol. 48, pp. 244-254, 2013.
[4] W. C. liu et al., *ISSCC*, pp. 182-183, 2017.
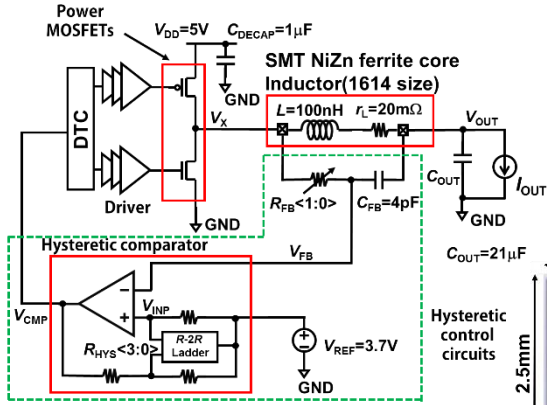[5] T. Nabeshima, et al, *PESC*, pp. 1711-1716, 2004.

Fig. 1 Circuit block diagram of the conventional hysteretic buck converter.

Fig. 2 COB implementation schemes. (a) WB and (b) FCB.
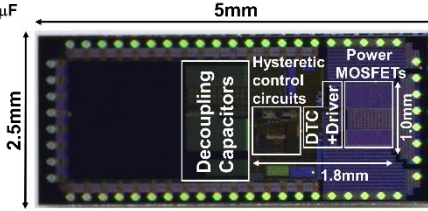
Fig. 3 Chip micrograph.
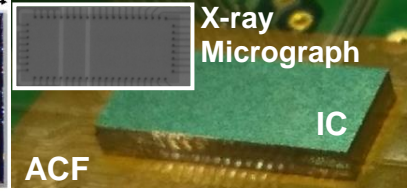
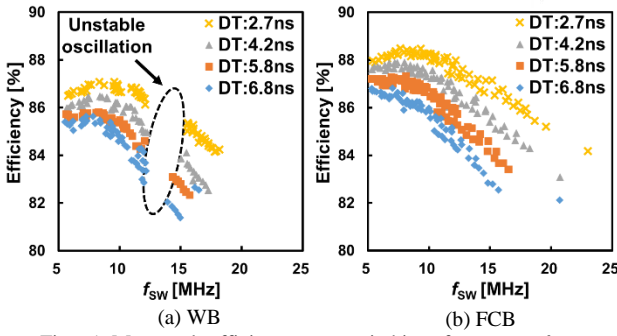Fig. 4 Photograph and X-ray micrograph of FCB implementation.

Fig. 5 Measured efficiency vs. switching frequency f_{SW} at I_{OUT}=800mA with various dead time (DT). (a) WB and (b) FCB.

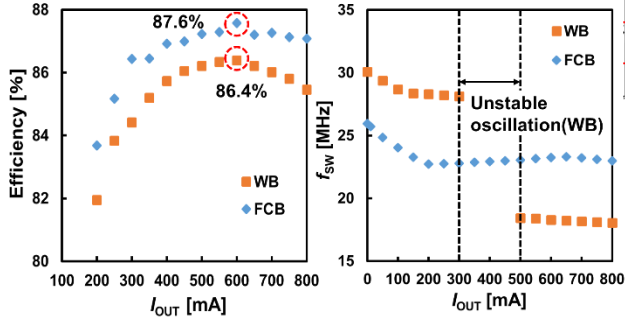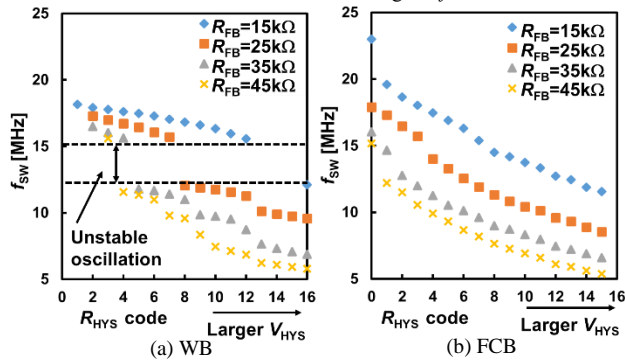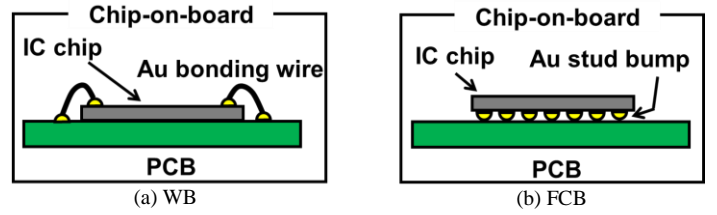Fig. 6 Measured efficiency vs. I_{OUT} at typical f_{SW} mode setting.

Fig. 7 Measured f_{SW} vs. I_{OUT} at the highest f_{SW} mode.
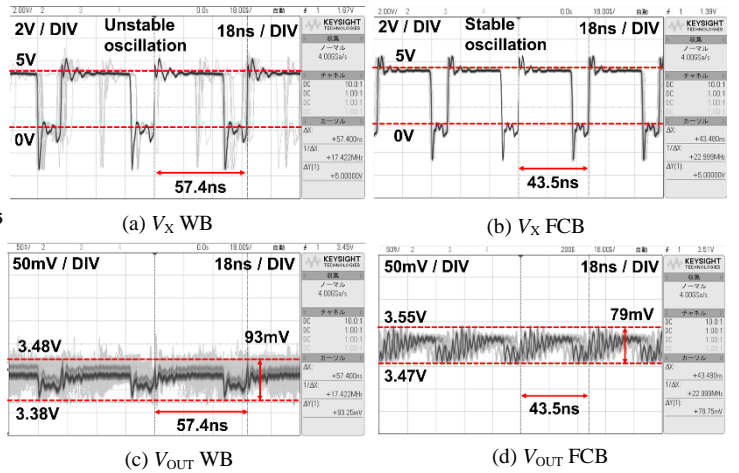

Fig. 8 Measured switching node voltage V_X and output voltage V_{OUT} waveforms at the highest f_{SW} mode. (a) V_X WB, (b) V_X FCB, (c) V_{OUT} WB and (d) V_{OUT} FCB.
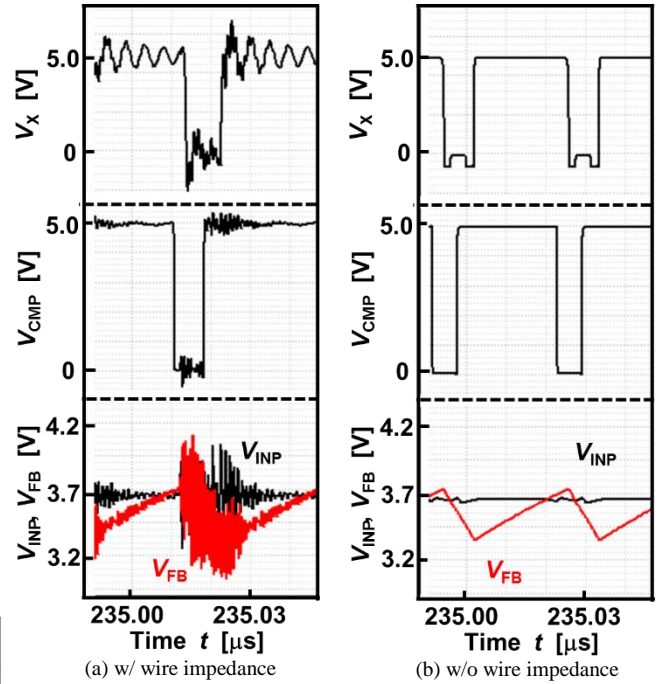

Fig. 9 Measured f_{SW} as a function of hysteresis window voltage V_{HYS} code (dead time 2.7ns, I_{OUT}=800mA). (a) WB and (b) FCB.

Table I Comparison table of WB and FCB.

	Max efficiency [%] @I_{OUT}=800mA	Max f_{SW} [MHz] @I_{OUT}=800mA	V_{OUT} ripple [mV] @I_{OUT}=800mA	Oscillation stability
WB	87.1 (f_{CLK}=8.34MHz)	18	93	Unstable
FCB	88.5 (f_{CLK}=7.65MHz)	23	79	Stable

Fig. 10 Simulated V_X, V_{CMP}, V_{INP}, and V_{FB} waveforms at the highest f_{SW} mode. (a) w/ wire impedance and (b) w/o wire impedance. Wire impedance of (50mΩ+1nH)/mm is assumed.