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A Compact Size, Wide-Range Efficiency, and Self-biasing CMOS-IPD Rectenna Using 2.5D Wafer-level Packing for a Biomedical Wireless Power Transfer System

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Abstract

This work achieves a two-and-a-half-dimensional (2.5D) wafer-level rectenna module with a compact size and high power conversion efficiency (PCE) that integrates a receiver coil in an integrated passive device (IPD) and a rectifier in a tsmc™ 0.18 μm CMOS process. The proposed rectifier provides a cross-coupled voltage doubling full-wave topology which can reach relatively high PCE by means of a relatively simple circuitry. The IPD receiver coil was stacked on top of the CMOS rectifier. The rectenna (including a receiver coil and rectifier) achieves an output voltage of 1.5 V and PCE of 74 % with a transmission distance equal to 3.5 cm. The PCE of the circuit maintain 73 % with 7 dB extension input power. The die size of the rectenna module is less than 0.7 cm^2, and is thus very suitable for wearable and implantable device over short ranges.

1. Introduction

Implantable biomedical devices demand a continuously available power source in vivo detection and treatment of various diseases, diagnostic and a variety of monitoring applications [1]. For a long lifetime, implanted batteries have fixed energy density in which has limited lifetimes and large size. However, a wireless power transfer (WPT) scheme is self-powering technology of remotely powered devices which recharges the batteries [2]. The powered devices have the advantages of a small form factor, low cost, easier deployment plan and better flexibility compared with batteries. WPT systems can harvest the radio frequency (RF) energy in a reader and then convert the short range transduced RF energy into an electrical AC signal. This technique thus provides a promising method to maintain a wireless power supply from an ambient RF electromagnetic field. In the frequency selecting, the wireless power link operates at 13.56 MHz which increases the power transfer efficiency by three times [3].

One of the most critical components in the WPT system is the rectifier circuit which is used for converting alternating current (AC) power to direct current (DC) power. The power conversion efficiency (PCE) of the rectifier can significantly influence the overall efficiency and performance of the system. PCE represents the quality of the rectifier and is expressed as (1).

$$PCE(\%) = \frac{V_{out}^2}{P_{IN} \cdot R_L} \times 100 \quad (1)$$

Where, V_{out}, R_L, P_{IN} are the DC output voltage, load resistance and input power, respectively. Various works have proposed different methods of improving the PCE of rectifiers. For example, an active rectifier compose two cross-coupled PMOS transistors and two comparator controlled NMOS switches which modify peak-current biasing circuit to operate efficiently over wide input amplitude and load current range. At 13.56 MHz operation, the PCE of proposed rectifier are 82.2 % to 90.1 % with ranges from 1.5 to 4 V for R_L=500 Ω [4]. A cross-coupled CMOS switches rectifier use multiplier configuration and dynamic body biasing circuit to reduce time delay which come from parasitic series resistance and shunt capacitance at each stage. The maximum PCE achieve 86.4 % at 13.56 MHz and 1 kΩ output load resistance [5].

This work proposes a compact and efficient rectifying circuit with a wide-range, self-biasing scheme, can avoids the reverse conduction problem and extend peak PCE over wide output voltage which the rectifier maintains 73 % with 7 dB extension input power. The rectifying circuit can achieve relatively high PCE by means of relatively simple circuitry, to feed the wireless power transfer rectenna module.

2. 2.5D wafer-level RF harvesting module Design

As shown in Fig.1, the proposed rectifier provides a cross-coupled voltage doubling full-wave topology, which primarily includes the four rectifying transistor and self-biasing cell. When the AC power is a positive half cycle, the electronic switch transistor (M_2) and diode-wired NMOS (M_3) will first become conductors and the direction of electric current flows into output node (V_{out}) via MN4 and discharge the DC voltage of V_L through M_2. The output voltage of the proposed rectifier is expressed as (2).

$$V_{out} = V_H - V_L = 2(A - V_d) \quad (2)$$

Where A and V_d are the input voltage amplitude and threshold voltage of NMOS. During the other half of the cycle, the electronic switch transistor (M_1) and the diode-wired NMOS (M_4) will first become conductors, and the current has the same direction as previous cycle of the output node (V_{out}) and V_L. At this time, the DC output voltage of V_{out} reaches 2(A-V_d). At low output DC voltage, the self-biasing cell (M_5 and M_6) are off. When the DC output voltage is high, the self-biasing cell will become a conductor which is derived from the DC voltage to the gate of the NMOS (M_3 and M_4) to reduce transistor's reverse leakage. The output voltage of the proposed rectifier is expressed as (3).

$$V_{out} = 3(A - V_d) \quad (3)$$

With the differential phase division switching achieved by the electronic switches, the DC voltage and PCE of the rectifier can both be improved. The receiver coil use a thin-film process

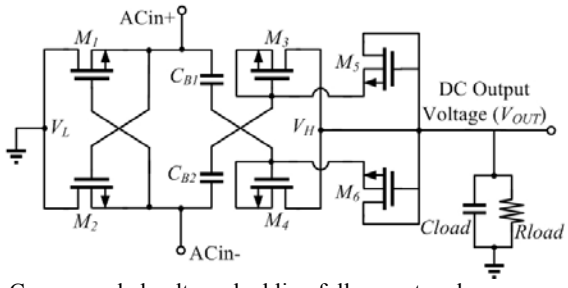

Fig. 1 Cross-coupled voltage doubling full-wave topology.

of IPD technology to built on a silicon substrate which can be used as a platform to bridge the Si interposer integration (2.5DIC) between the assembly substrate and integrated CMOS circuit. The assembly CMOS-IPD technology reduces the dielectric loss of passive components and optimizes the system performance and cost.

3. Measurement Results

The proposed CMOS-IPD circuit was designed and fabricated using the tsmc^{TM} 0.18 μm CMOS process and an IPD technology. The circuit was simulated using the Agilent Advanced Design System^{TM} (ADS) simulator. Figure 2 (a) shows a chip photo of the CMOS-based rectifier without an IPD antenna, whose chip size is 0.31 mm^2, including the bump pads. Figures 2 (b) and (c) show the side and isometric views of the assembled CMOS-IPD module; the antenna is mounted with solder bumps at a height of 70 μm between the CMOS chip and the IPD substrate. Figure 2 (d) shows a photograph of the IPD coil and IPD interconnects. By rectifying the RF power test, includes a coupling coils on single-side printed circuit boards (PCBs) transmitting at a power level of 1W which will transmit the RF energy to the CMOS-IPD rectenna system in Fig.3. The wireless transmission distance is between 1cm and 5 cm, the PCE and DC output voltage of the rectenna versus the input power from -13 dBm to 8 dBm. The rectenna achieves an output voltage of 1.5 V and PCE of 74 % with -7 dBm input power. The measured results show the maximum efficiency of 82 % and maintain 73 % with 7dB extension input power. Table I present the overall performance of recently published RF rectenna designs, and previously published 13.56 MHz rectennas [3-4], [6-7].

4. Conclusion

This work validated an efficient rectifying circuit, in which a cross-coupled voltage doubling full-wave topology is achieved with a relatively simple circuitry. Its function provides the differential phase division switching and self-biasing cell that avoids the reverse conduction problem and extend peak PCE. This circuit uses a CMOS-IPD technology which integrated an IPD receiver coil was successfully developed to fabricate 2.5D wafer-level RF harvesting rectenna module for wireless power transfer system. With a Wireless transmission distance equal to 3.5 cm, the measured results of output voltage and PCE were 1.5 V and 74 %, respectively. The die size of rectenna module is less than 0.7 cm^2, and is thus very suitable for wearable and implantable device over short ranges which can be blended in with any home or office environment.

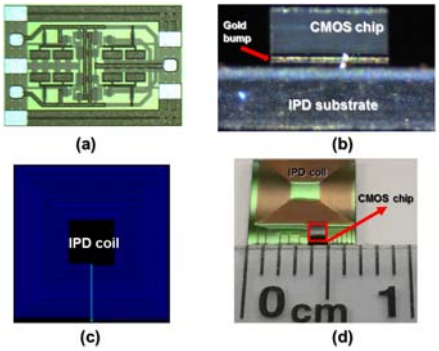

Fig. 2 Photographs of the rectenna with IPD. (a) CMOS rectenna without IPD, (b) the side view of the CMOS-IPD rectenna, (c) the part of IPD, (d) the isometric view of the CMOS-IPD rectenna.

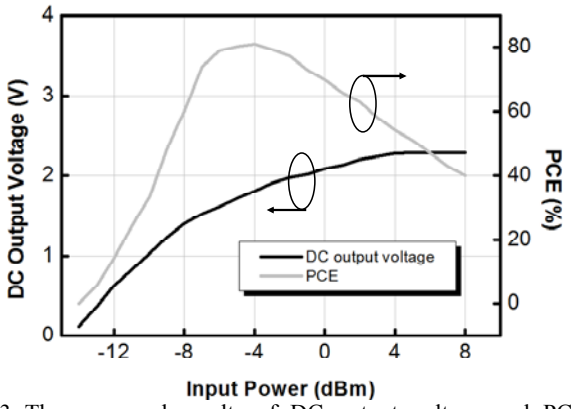

Fig. 3 The measured results of DC output voltage and PCE of rectenna.

Table I Performance benchmark against previously reported results

Ref.	Freq. (MHz)	Coil diam. (cm)	Output voltage (V) at Input power	PCE (%)
[3]	13.56	0.7	1.2 @ 120 mW	N/A
[4]	13.56	2	1.19 @ 30 mW	82.2
[6]	13.56	N/A	1.8 @ 0.96 mW	68
[7]	13.56	N/A	2 @ 47 mW	85
This work	**13.56**	**3.5**	**1.5 @ 0.2 mW**	**74**

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