Extended Abstracts of the 2017 International Conference on Solid State Devices and Materials, Sendai, 2017, pp529-530

K-3-06 (Late News)

Dependence of Channel Mobility on Substrate Impurity Concentration for Metal Source/Drain Ge MOSFETs

Taisei Sakaguchi[1], Kentaro Akiyama[1], Keisuke Yamamoto[1], Dong Wang[1], and Hiroshi Nakashima[2]

[1]Interdisciplinary Graduate School of Engineering Science, Kyushu University
6-1 Kasuga-koen, Kasuga, Fukuoka 816-8580, Japan
E-mail: 2ES16031W@s.kyushu-u.ac.jp
[2]Global Innovation Center, Kyushu University
6-1 Kasuga-koen, Kasuga, Fukuoka 816-8580, Japan

Abstract

We investigated the relation between the substrate impurity concentration (N_I) and channel mobility (μ) for Ge MOSFETs. The source/drain regions of n- and p-MOSFETs were fabricated using TiN/Ge and PtGe/Ge contacts, respectively. For n-MOSFET, the electron μ in the lower electric field was largely increased with a decrease in N_I. For p-MOSFET, the increasing tendency was not observed, and the hole μ was limited ~200 cm^2/Vs. The N_I dependence of μ is explained in terms of Coulomb scattering by ionized charges in the gate stack and the ionized impurity underneath the channel.

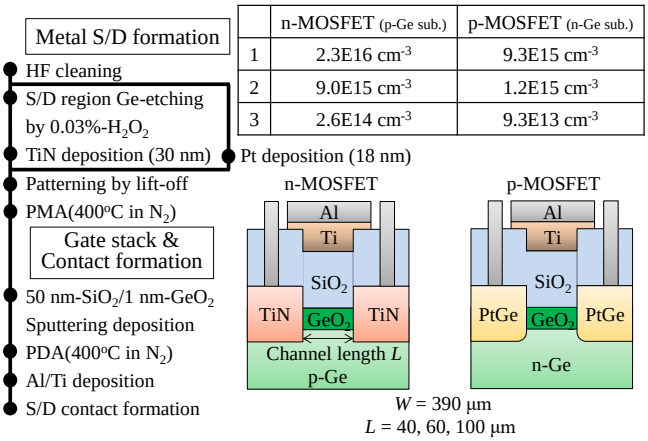
1. Introduction

Ge is of great interest as a candidate channel material for future CMOS devices owing to its high intrinsic carrier mobility. To translate its potential into scaled CMOS devices, an ultra-shallow S/D junction with very low sheet resistance should be achieved. However, it is difficult to satisfy these requirements using conventional doped S/D junctions because of the low solubility limits and large diffusion coefficients of the dopants in Ge. Metal S/D MOSFETs are a promising solution for these problems. We demonstrated the p-MOSFET operation using PtGe-S/D with a low hole barrier height of ~0 eV, indicating the low parasitic resistance (R_{PR}) of S/D [1]. We also demonstrated the n-MOSFET operation using TiN-S/D with a low electron barrier height of ~0.1 eV and succeeded in low R_{PR} using embedded S/D structure [2]. The peak channel mobilities for hole and electron were ~200 cm^{2}V^{-1}s^{-1}, which are lower than those of pn-S/D MOSFETs [3]. The high quality gate stacks with low interface state density (D_{it}) and low oxide fixed charge density (Q_f) are essential for enhancing the mobility. Besides, it is well known that the charged impurity underneath the channel is also affect the mobility (μ). However, the influence of charged impurity on μ regarding Ge MOSFETs is not investigated.

In this work, we focus on clarifying the influence of charged impurity on hole- and electron-mobilities for metal S/D n- and p-MOSFETs.

2. Experimental

Figure 1 illustrates our gate-last process for the metal S/D n- and p-MOSFETs. The substrates were (100) Ge with the impurity concentration (N_I) ranging from 10^{13} to 10^{16} cm^{-3}, details of which are listed in Fig. 1. The chip-size substrate was dipped in dilute HF solution followed by rinsing in DI water. Then, photoresist was coated and patterned for S/D region. For metal S/D of n-MOSFET, 20-nm-thick Ge was etched by using 0.03%-H_2O_2 to form embedded S/D. Then, a TiN film was deposited by rf sputtering and patterned as S/D by lift-off technique. Then, PMA was performed at 400°C for 30 min in N_2. Similarly, for metal S/D of p-MOSFET, a PtGe/Ge contact was formed using the same method mentioned above (Ge etching was cancelled). After cleaning by 0.1% dilute HF followed by DI water rinsing, the SiO_2/GeO_2 gate stack was formed by sputtering method [3]. After PDA at 400°C for 30 min in N_2, Al/Ti films were deposited and patterned as metal gate. After that, contact holes on metal S/D region were opened, and Al electrodes were formed by thermal evaporation and lift-off techniques. Finally, contact annealing was carried out at 300°C for 10 min in N_2. The Channel sizes in this work were a constant channel width (W) of 390 μm and 3 kinds of channel lengths (L) of 40, 60 and 100 μm.



	n-MOSFET (p-Ge sub.)	p-MOSFET (n-Ge sub.)
1	2.3E16 cm^{-3}	9.3E15 cm^{-3}
2	9.0E15 cm^{-3}	1.2E15 cm^{-3}
3	2.6E14 cm^{-3}	9.3E13 cm^{-3}

Fig. 1 Fabrication procedures for n- and p-MOSFETs with metal S/D structure.

3. Results and discussion

Figures 2(a) and 2(b) show the representative drain current (I_D) vs drain voltage (V_D) characteristics for n- and p-MOSFETs, respectively. The channel conductions are well controlled by the gate voltage (V_G), implying that the PtGe/Ge and TiN/Ge contacts work well as S/D. Figures 3(a) and 3(b) show the source current (I_S) vs V_G characteristics for 3 kinds of N_Is for n- and p-MOSFETs, respectively. It was found that I_S under OFF state increases with a decrease in N_I. This is due to an increase in the minority carrier density with decreasing N_I [4].

In order to evaluate R_{PR}s for n- and p-MOSFETs, total

resistance (R_{total}) and L are plotted, which are shown in Figs 4(a) and 4(b), respectively [5]. From extrapolated y-interception, R_{PR}s were estimated as ~250 Ω and ~130 Ω for n- and p-MOSFETs, respectively. These low R_{PR} values are comparable to our previous report [2].

The field effect mobility (μ_{FE}) was evaluated using the I_S-V_G data with the relation $\mu_{FE} = g_m/[(W/L)C_{OX}V_D]$ [5]. Here, g_m is the transconductance, and C_{OX} is the gate capacitance which is experimentally obtained from the gate-channel capacitance from split C-V measurement. Figures 5(a) and 5(b) show μ_{FE} as a function of V_G for n- and p-MOSFETs with 3 kinds of N_Is. The peak electron μ_{FE} in low-V_G region is increased with a decrease in N_I for n-MOSFETs, as shown in Fig. 5 (a). On the other hand, the peak hole μ_{FE} is limited to ~200 cm^2/Vs, as shown in Fig. 5 (b), and the N_I dependence is weaker than that of n-MOSFET. Generally, mobility degradation in the low-V_G (or low-field) region is dominated by Coulomb scattering caused by the D_{it} and Q_f in the gate stack, and ionized impurities underneath a channel [6]. It is clear from the n-MOSFET results that the Coulomb scattering by D_{it} and Q_f is weaker than that by the ionized impurities. On the other hand, the Coulomb scattering of hole in the p-channel is governed by D_{it} and Q_f. The schematic diagrams of limiting factor for n- and p-MOSFETs are shown in Fig. 6(a) and 6(b). In order to investigate the influence of N_I on hole mobility of Ge p-MOSFET, it is necessary to reduce Coulomb scattering in the gate stack using defect termination technique such as Al-PMA effect [7].

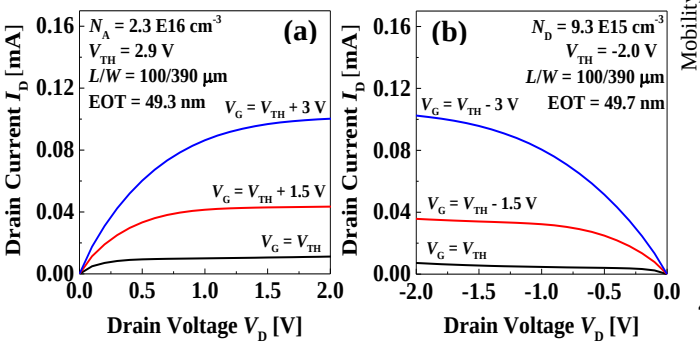


Fig. 2 I_D-V_D characteristics for typical (a) n-MOSFET (b) p-MOSFET.

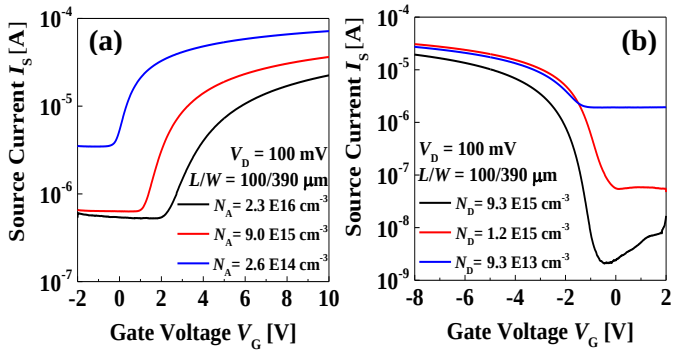


Fig. 3 I_S-V_G characteristics for (a) n-MOSFETs (b) p-MOSFETs.

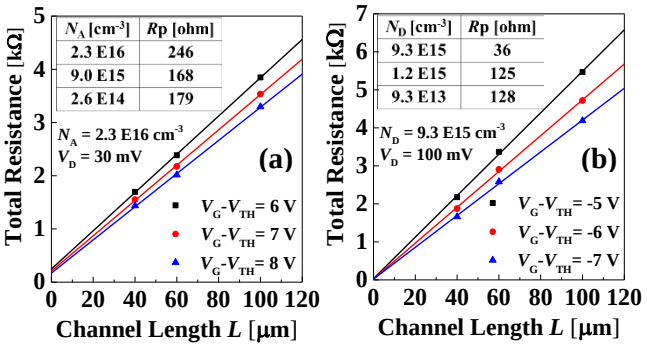


Fig. 4 Relationship between R_{total} and L for (a) n-MOSFETs (b) p-MOSFETs. R_{PR}s for all samples are also listed in the tables in each figure.

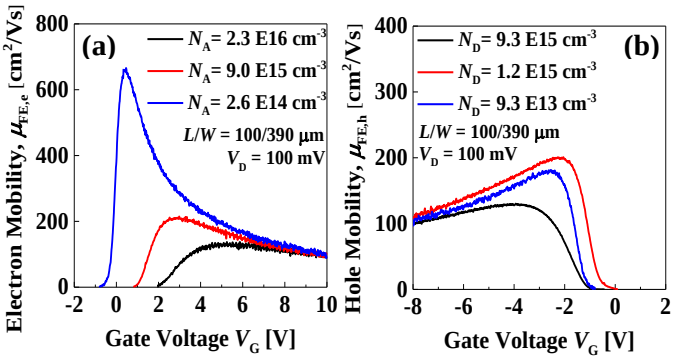


Fig. 5 μ_{FE}-V_G plots for (a) n-MOSFETs (b) p-MOSFETs.

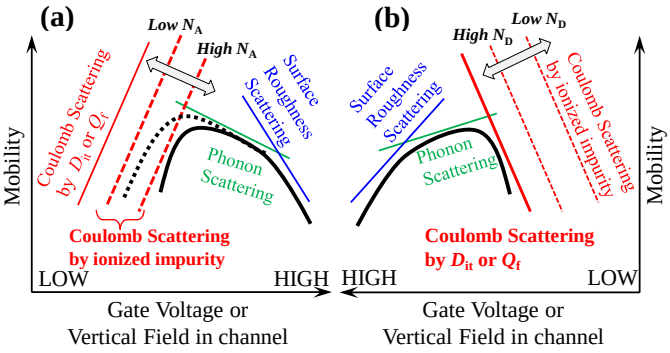


Fig. 6 Schematic model of mobility degradation mechanism for (a) n-MOSFET and (b) p-MOSFET.

4. Conclusions

We investigated the N_I dependence of channel mobility for metal S/D Ge MOSFETs. The peak μ_{FE} of n-MOSFETs showed the strong dependence on the N_I, but the μ_{FE} of p-MOSFETs showed almost no dependence on the N_I. The N_I dependences of μ_{FE}s could be explained in terms of Coulomb scattering by ionized charges in the gate stack and the ionized impurity underneath the channel.

References

[1] Y. Nagatomi *et al.*, JJAP **54**, 070306 (2015).
[2] Y. Nagatomi *et al.*, Semicond. Science Technol. **32**, 035001 (2017).
[3] K. Yamamoto *et al.*, APEX **4**, 051301 (2011).
[4] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. p.166.
[5] D. Schroeder, *Semiconductor Material and Device Characterization*, 3rd ed.
[6] S. Takagi *et al.*, IEEE EDL **41**, 2357 (1994).
[7] Y. Nagatomi *et al.*, Mat. Sci. in Semicond. Process. in press (doi: 10.1016/j.mssp.2016.11.014).