Extended Abstracts of the 2017 International Conference on Solid State Devices and Materials, Sendai, 2017, pp531-532

K-4-01 (Invited)

Ion implantation technology for advanced ULSI devices

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Abstract

The evolution of ion implantation applications and equipment technology for advanced ULSI will be discussed. The main topics will be these technologies' applications to the most advanced CMOS. Technological insights for emerging devices will also be discussed.

1. Introduction

Starting from early 1970s, ion implantation technologies have been the industries' standard for semiconductor device fabrications. With respect to doping, ion implantation techniques are still key process technologies as of today [1]. Ion implantation technologies keep evolving its performance to realize continuous scaling of device size and to improve device performance. After the introduction to Vth adjustment with a capability of accurate dose and energy control, ion implantation was expanding its application area such as low-energy high dose implantation for source/drain formation, high-energy ion implantation for retrograde-well formation, ultra-high energy implantation for CMOS imager. These technologies significantly contributed to the improvement of the performance and the productivity of LSI.

Continuous efforts and resources are devoted to achieve more precise doping (dose, energy, angle, damage, contamination) from demanding specifications requests by the device scaling requirements. Recently, ion implantation technologies are faced with new challenges, since 3D structurer such as Fin-FET and DTI, and novel channel materials such as SiGe, Ge and III-V materials are adopted for advanced devices applications. In this paper, I will discuss ion implantation technologies from the viewpoints of applications and equipment.

2. Ion Implantation Technologies

Figure 1 summarizes the application of ion implantation. Almost all of the doping steps for CMOS fabrication are covered by ion implantation processes. The energy range from 100eV to 5MeV corresponds the projected range from surface to several um depth in Si. This wide range of depth in substrates makes it a versatile production tool. Ion implantation technique can introduce dopant into substrates exactly at desired depth with desired concentration.

2.1 Doping for advanced transistors

To suppress the short channel effect and to reduce the parasitic resistance of the transistor, shallow and abrupt junction with low resistivity is strongly required. Various approaches including the decrease in implantation energy have been investigated to form a shallow dopant profile.

a) Co-implantation

Various ion species are used to control dopant profile. Si and Ge ions are utilized for pre-amorphization to prevent a channeling of dopant. C, F and N ions are co-implanted with dopant based on their unique characteristics which include dopant diffusion control, suppression of secondary defects, reduction of interface states, and suppression of hot-carrier immunity [2],[3]. Co-implantation technology also utilized stress enhancement to enhance channel mobility of MOSFETs.

b) Damage control

Residual defects induced by ion implantation causes to increase in the junction leakage current. There are many thermal solutions from the annealing process to overcome this issue. Ion implantation processes also play important role for defect control. Cold implantation can create a thicker amorphous layer [4]. Therefore, end of range defects can be reduced in addition to the high activation rate compared with RT implantation. Hot implantation can also minimize defect generation in the relatively low dose area due to the dynamic annealing mechanism [5]. The appearance of patterning material with high temperature resistance accelerates this application.

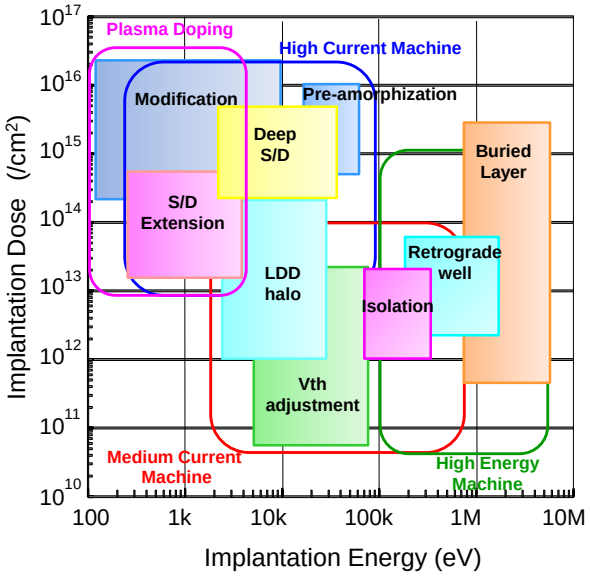

Fig. 1 Application of ion implantation

c) Precise angle control

The increase in variability becomes a serious issue for a scaled LSI. It results in the decrease in static noise margin of SRAM and the small sensing margin of sensing amplifier circuit. The precise control of parallelism and incident angle of ion beam in leading edge implanters minimize the angle variation within wafer. This improvement contributes to the symmetrical source/drain formation and the reduction of variation of transistor characteristics. The precise angle control also enables the channeling implantation. The deeper profile is realized by channeling implantation with same resist thickness for random direction implantation. The increase in beam divergence is a big problem in high beam current with low energy application. The ion beam easily spreads by space charge. The cluster ion implantation such as using $B_{10}H_{14}$, $B_{18}H_{22}$ can reduce the beam divergence since equivalent energy of these cluster ions is high and the amount of charge is small, compared with that of monomer ion [6].

2.2 Doping for Ge substrate

The current high performance transistor aspirations are for high-mobility channel, like strained silicon, strained SiGe, Ge and III-V materials. Among group IV elements, Ge offers a 4 times higher hole and a 2.5 times higher electron mobility than Si. However several challenges still remain for the fabrication of Ge MOSFETs. For junction formation, it is difficult to form shallow N^+/P junction in Ge due to the anomalous high diffusion coefficient of donor ions. To address these problems, some processes have been proposed such as aluminum co-doping, group-III metal doping [7],[8]. Alternatively, forming shallow P^+/N junction is relatively easy. However the high activation of acceptor ions is difficult. Controlling the oxygen atom at surface region by the pre-heating the substrate in vacuum before implantation is effective to realize shallow P^+/N junction with low resistivity [9].

2.3 Doping for 3D structure

The demand of conformal doping rapidly increases due to the introduction of 3D structures such as Fin-FET and deep trench isolation (DTI) into advanced ULSI. It is very difficult to realize conformal doping by using a conventional beam line implantation. Plasma doping is the most promising candidate for conformal doping [10]. Sidewall doping of Fin and DTI can be realized utilizing the collision effects by control of the substrate bias and gas pressure. In addition to this feature, extreme shallow dopant profile can be formed by this technique with high productively. Furthermore, high aspect ratio doping such as bottom area doping of DTI can be realized by plasma doping. The directional doping with small beam divergence by changing the process parameter meets this requirement.

2.4 Doping for next generation power devices

SiC and GaN devices are targeted as a next generation power devices. Novel ion species are required for these devices. For SiC devices, high temperature AL implantation is required to reduce the residual defects. Mg ion for source implantation, and Fe or Ar ion implantation for isolation are required in GaN device fabrication process.

2.5 Productivity and yield control

The productivity of ion implanter has been improved in two major ways, increasing in the mechanical throughput of wafer handling and the enhancement of the beam current. The increased versatility of the dose and energy between medium current, high current and high energy machines expands the flexibility of production. Advanced process control (APC) has been adopted into ion implantation step to enhance the device yield. Implantation dose of each wafer can be varied from that of a previous process step. Implantation dose within a wafer can also be changed to compensate the non-uniformity of the oxide thickness and/or the gate length of Tr. With this technique, the variation of transistor characteristics can be minimized.

2.6 Perspective of ion beam process

The increase in beam current of implanter enables the high dose implantation with more than 1E16 /cm^2. This improvement turns surface modification application in reality. Highly doped materials change its original property.

Ion beam etching is one of the candidates for patterning of magnetic tunnel junction (MTJ) of MRAM as an emerging device.

3. Conclusions

The evolution of ion implantation technologies was reviewed. The successive innovations for both process control and ion implanters realized new features and higher performances consecutively in semiconductor devices. The further development of this technology will contribute to the improvement of emerging devices.

Acknowledgements

Author would like to express his sincere thanks to Drs. S. Sakai, T. Nagayama, N. Tokoro, T. Ikejiri, N. Hamamoto and M. Naito of Nissin Ion Equipment Co.,Ltd. for helpful discussion throughout this work.

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