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CMOS Compatible Ferroelectric Devices for Beyond 1X nm Technology Nodes

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Abstract – 10 years have passed since ferroelectricity in hafnium oxide was discovered for the first time. This fundamental breakthrough has initiated significant R&D activities in both industry and in academia. This paper summarizes the potential of ferroelectric HfO_2 (FE-HfO_2) for memory applications with particular focus on highly scaled CMOS technology nodes. It illustrates that FE-HfO_2 might finally enable the entrance of ferroelectric memories into mass markets.

1. Introduction

In 2007, ferroelectric properties were discovered in silicon substituted hafnium oxide (Si:HfO_2) at former DRAM manufacturer Qimonda AG [1]. In 2011, first publications appeared that assigned these unexpected physical properties to the stabilization of an intermediate, non-centrosymmetric, orthorhombic crystal phase [2]. In the following years a wave of research activities was triggered culminating in several proof-of-concept demonstrations (all based on FE-HfO_2) which are listed in the following:

Table I FE-HfO_2-based proof-of-concept demonstrations

Device type	Replacement	Ref.
Nonvolatile FeFET	NVM	[3]
3D ferroelectric capacitors	FRAM	[4]
Volatile FeFET	SRAM / DRAM	[5]
Negative Capacitance FET	MOSFET	[6]
Monolithic ferroelectric device	Passive comp.	[7]
Versatile FeFET	MOSFET+DRAM	[8]
Ferroelectric Tunnel Junction	NVM / SCM	[9]
FeFET synapse	CMOS	[10]
FE-based solar cells	Solar cells	[11]
FE-based HF devices	Filters etc.	[12]
3D FeFET NAND	SSD	[13]
Pyroelectric sensor	IR sensors	[14]
Radiation hard capacitors	FRAM	[15]

Accordingly, numerous application areas might benefit from the discovery of ferroelectricity in hafnium oxide in the future. The major drivers for the exponential increase in research activities on FE-HfO_2 are manifold:

- CMOS compatibility of HfO_2
- FeFETs can be derived from HKMG MOSFETs
- Conformal deposition of HfO_2 via ALD (3D)
- FE-HfO_2 as lead-free ferroelectric
- High confidence level of industry in HfO_2
- Ferroelectricity represents an ideal memory effect
- Thin film capability (sub 10 nm)

Summarized, FE-HfO_2 can resolve the major obstacles that have puzzled classical perovskite-type ferroelectrics. As an example, the classical ferroelectric PZT suffers from significant limitation with respect to material complexity, CMOS compatibility and scalability. The following sections will summarize how FE-HfO_2 might lead into a new age of ferroelectric devices with particular focus on the memory space.

2. The Next Generation of 1T-1C FRAM

Classical ferroelectric memories are based on a one transistor-one capacitor (1T-1C) architecture in which the state of the ferroelectric is destructively read, very similar to DRAM (even though not identical). That causes stringent requirements with respect to the cycling endurance of the ferroelectric which could indeed be met after many years of development. The main reason however why FRAM could never fulfill its original vision (replacing Flash altogether) was due to the fact that the capacitor has remained a planar one ever since the introduction of FRAM. DRAM has faced that same problem in the past and could extend its lifetime until today by moving the capacitor into the third dimension (trench and stacked capacitors). In the past, performing the same transition for ferroelectric capacitors was never successful due to the fact that a conformal deposition of perovskites could not be demonstrated [16].

For FE-HfO_2, that problem is not present anymore since the material is a rather simple binary oxide and mature ALD process technologies exist. Accordingly, 3D ferroelectric capacitors could successfully be demonstrated in 2014 [4]. Hence, any advanced manufacturer with an established trench or stacked capacitor process technology could make use of this material innovation. Consequently, new types of NV-RAM products can be envisioned even at the latest 1X nm DRAM technology nodes [17].

3. The Ideal Ferroelectric Memory Cell: The FeFET

Even though FE-HfO_2 could resolve some of the major roadblocks for further FRAM adoption, the fundamental problems that arise from the 1T-1C architecture remain:

High cost due to 3D capacitor module, high endurance requirements due to destructive read out, limited scalability beyond 1X nm technology node, limited access speed due to high plate line capacitance.

A solution to these limitations is given by the ferroelectric field effect transistor (FeFET). In the FeFET, the gate insulator of a standard MOSFET device is replaced by a ferroelectric thereby giving the transistor nonvolatile memory properties (see Fig. 1).

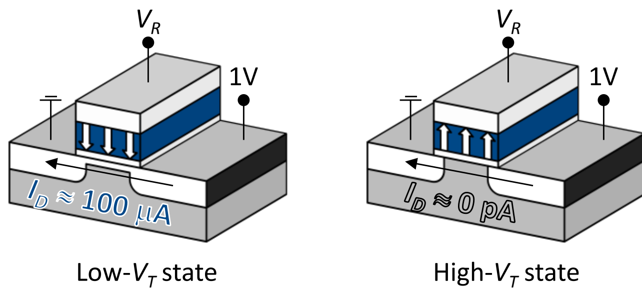

Fig. 1 FeFET memory cell (left: "ON" state; right: "OFF" state) during read out. Depending on the polarization of the memory cell high or no drain current I_D flows when a read voltage V_R is applied to the gate. The binary states are nonvolatile similar to Flash memory cells.

This device can resolve all remaining problems of 1T-1C based FRAM by moving to 1T FeFET: Minimal cost overhead (only 2 additional lithography steps) [18], non-destructive read-out and access speed even higher than classical embedded Flash (due to a higher gate stack capacitance). Even more importantly, due to the fact that hafnium oxide is currently the state-of-the-art gate dielectric in all 2X nm, 1X nm and most likely all future 0X nm nodes, any FET can be turned into an FeFET.

4. Scalability of FeFET-based Memories

Due to the inherent compatibility of FE-HfO_2 to high-k metal-gate process technology, the FeFET has the potential to be implemented on literally any advanced CMOS baseline (see Fig. 2).

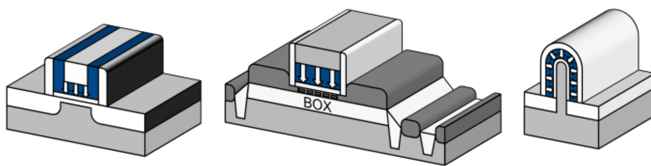

Fig.2 Alternative implementations of FeFET memory cells. Illustrated are gate last (left), fully-depleted-silicon-on-insulator (middle) and FinFET (right) implementations.

Accordingly, planar gate last implementations can be performed as well as implementations for fully-depleted-silicon-on-insulator (FDSOI) platforms. Especially the combination of FDSOI and FeFET can be considered ideal: The FDSOI process platform is in general optimized for cost and low-power which are also some of the major differentiators of the FeFET concept compared to other emerging memory concepts: The FeFET memory technology adds only negligible overhead to the CMOS baseline (cost) and the write operation is field and not current driven (low-power). More importantly, due to the possibility to write the FeFET cell via the source and drain regions [19], no dedicated bulk area is required for embedded FeFET cells.

And finally again due to its mature ALD process capability, there are already demonstrations on the FinFET capability of the FeFET concept [20]. This allows for envisioning the FE-HfO_2-based FeFET concepts down to 0X nm device architectures like nanosheets [21].

5. Conclusions

An overview on the R&D activities triggered by the discovery of ferroelectricity in hafnium oxide was given. Focusing on memory applications it can be stated that FE-HfO_2 might lead to fundamental changes to classical FRAM as well as it might finally lead to the introduction of the FeFET memory cell into mass markets. Due to its close relation to high-k metal-gate process technology, the FE-HfO_2-based FeFET shows great potential to impact semiconductor industry over the next decades.

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