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Guiding principles for the fabrication of V-MOSFETs based on a Si emission model

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Abstract

It is expected that the off-state leakage current of MOSFETs can be reduced by employing Vertical Body Channel MOSFETs (V-MOSFETs). However, in fabricating these devices, the structure of Si pillars sometimes cannot be maintained during oxidation, since Si atoms are sometimes emitted from the Si/oxide interface (Si missing). Thus, in this study, we utilized a Si emission model to investigate the thermal oxidation of Si with various surface orientations. We used first-principles calculations based on density functional theory. The results show that the order in which Si atoms are more likely to be emitted during thermal oxidation is (111)>(110)>(310)>(100). Moreover, the emission of Si atoms increases as the compressive strain increases. Therefore, the emission Si of atoms occurs more easily in V-MOSFETs than in planar MOSFETs. To reduce the Si missing in V-MOSFETs, oxidation processes that induce less strain, such as wet or pyrogenic oxidation, are necessary.

1. Introduction

The progress in electronic circuits has been accomplished by downscaling MOSFETs. However, downscaling has led to an increase in off-state leakage current. It is expected that the all around gate structure of Vertical body channel MOSFETs (V-MOSFETs) will enable the leakage current to be reduced (Fig.1). A further advantage is that V-MOSFETs can be integrated more easily than conventional planar MOSFETs. To fabricate these devices, it is necessary to oxidize Si pillars. However, the structure of these pillars cannot sometimes be maintained during oxidation because Si atoms at the Si/oxide interface can be emitted as shown in Fig.2 (Si missing). This phenomenon can have a damaging effect on device characteristics.

In our previous work, it was shown that Si atoms are spontaneously emitted to release the strain induced by thermal oxidation, as shown as Fig.3, and that this was crucial during thermal oxidation [3]. In a Si pillar the interface has various orientations. Thus, we investigated the dependence of strain on the orientation of the interface during thermal oxidation, and the effect this has on the emission of Si atoms.

2. Methodology

In this study, we used first-principles calculations based on density functional theory. The calculations were performed using the VASP code with the PBE generalized gradient approximation [4]. The core valence interactions were described by PAW potentials. k points were sampled with a 5×3×1 Monkhorst-Pack grid with integration over the Brillouin zone. The cutoff energy was 500eV. The Si/SiO_2 slab models used in this study are shown in Fig.4.

First, we simulated the oxidation process by inserting O atoms into the Si-Si bonds at Si/SiO_2 interfaces with various orientations. Since oxidation of a Si pillar induces strain due to the volume expansion of the SiO_2 (Fig.5), we took this into account by applying compressive strain in the x-y plane and tensile strain along the z axis (in the direction of the pillar) to models of Si/SiO_2 interfaces with a Poisson ratio of 0.3.

3. Results

In Fig.6, we show the calculated results. ΔE_{emit} is the change in total energy after the emission of a Si atom. When ΔE_{emit} is positive value, the Si emission doesn't occur. Whereas, when ΔE_{emit} is negative value, the Si emission occurs. This graph shows that ΔE_{emit} decreases as the areal density of the O atoms increases. At the areal density of O atoms becomes 0.031, 0.051, 0.096, 0.154 $[\text{Å}^{-2}]$ at Si(111)/SiO_2, Si(110)/SiO_2, Si(310)/SiO_2, and Si(100)/SiO_2 interfaces, respectively, ΔE_{emit} becomes zero. A decrease in ΔE_{emit} corresponds to an increase in the emitting number of Si atoms. Thus, the strain at the Si/SiO_2 interface increases as O atoms are inserted. However, the Si emission rate during thermal oxidation depends on the orientation. The order is $(111) > (110) > (310) > (100)$. This orientation dependent Si emission rate leads to the orientation dependent oxidation rate, resulting in the non-uniform V-MOSFET oxidation and non-circular channel shape. Moreover, by investigating the atomic structure at the interface, we found the order in which strain accumulates is $(111) > (110) > (310) > (100)$.

Fig.7 shows the compressive strain dependence for $Si(100)/SiO_2$ and $Si(110)/SiO_2$ interfaces. ΔE_{emit} increases as the strain increases in both two cases as shown in Fig.8. This indicates that compressive strain enhances the Si emission at the Si/SiO_2 interfaces the same as in the case of our previous works of Si(100)/SiO_2 interfaces [5]. This corresponds to the enhancement of Si missing by the strain. Thus, Si missing occurs more easily in V-MOSFETs than planer MOSFET, since the strain due to oxidation in V-MOSFETS is larger than in planar MOSFETs . ΔE_{emit} of $Si(110)/SiO_2$ decreases more significantly than that of $Si(100)/SiO_2$. Thus, the emission of Si occurs more easily in Si pillars than Si planer as the interface in the pillars has Si(110).

To prevent the Si missing in the fabrication processes of V-MOSFET, it is necessary to use an oxidation process that induces lower strain, such as wet or pyrogenic oxidation. (Fig.9)

4. Conclusion

We used a Si emission model to examine the thermal oxidation of Si and investigate the emission of Si atoms in fabricating V-MOSFETs. We found that the strain at the Si/SiO_2 interface accumulates as O atoms are incorporated during oxidation. The emission of Si atoms occurs more easily in V-MOSFETs than in planar MOSFETs because compressive strain tends to be introduced into the V-MOSFET. To prevent the emission of Si atoms, an oxidation process that induces smaller strain, such as wet or pyrogenic oxidation, is needed.

Acknowledgements

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References

[1] T. Endoh, K. Sakui, and Y. Yasuda, IEICE Trans., **E93-C**, 557 (2010).
[2] H. Kageshima, K. Shiraishi , and T. Endoh, Jpn. J. Appl. Phys. **55**, 08PE02 (2016).
[3] H. Kageshima and K. Shiraishi, Phys. Rev. Lett. **81**, 5936 (1998).
[4] G. Kresse and J. Hafner, Phys. Rev. B **47**, 558, (1993).
[5] S. Kawachi et al. ECS Transaction **75**, 293 (2016).

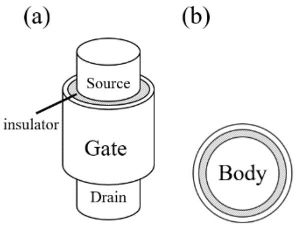

Fig.1: Vertical body channel MOSFET with all around gate structure. (a) Schematic of V-MOSFET. (b) Cross sectional view of the channel. [Ref. 1]

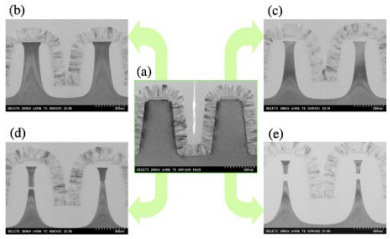

Fig. 2: Typical experimental results showing cross-sectional TEM images for (a) the initial stage, (b) 130 nm oxidation, (c) 190 nm oxidation, (d) 250 nm oxidation, and (e) 290 nm oxidation. [Ref. 2]

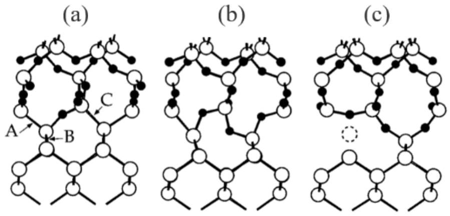

Fig.3: Side views of the Si/SiO_2 interface for studying accumulation and the release of the stress. The filled circles are O atoms, the clear circles are Si atoms, and the broken circle is the position from which a Si atom has been ejected. (a) interface with a low-stress quartz-like oxide. (b) interface before ejection. (c) interface after ejection [Ref. 3].

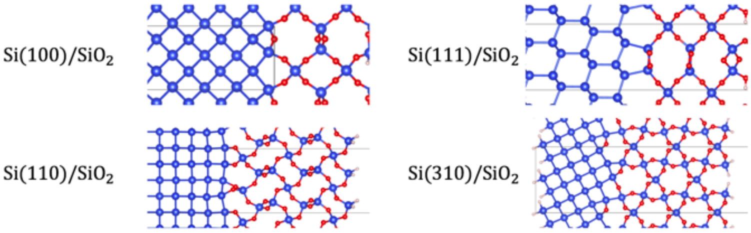

Fig.4: Slab models of $Si(100), (110), (111), (310)/SiO_2$ interfaces. The blue circles, red circles, and white circles correspond to Si and O and H atoms, respectively.

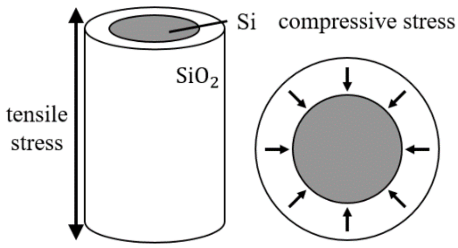

Fig.5: Both tensile and compressive stresses are induced by the oxidation of Si pillars.

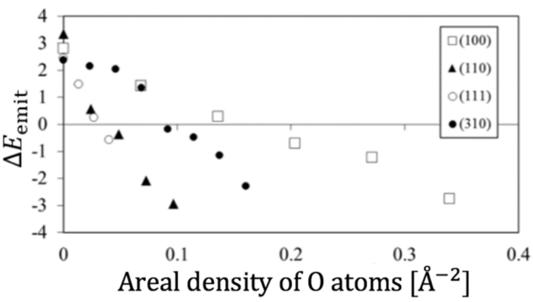

Fig.6: Energy change after the ejection of a Si atom during oxidation of the Si/SiO_2 interface. ΔE_{emit} is defined as follows:

$$\Delta E_{emit} = (E_{after\ emission} + E_{Si\ atom}) - E_{before\ emission}$$

$E_{after\ emission}$ is the energy of the system after emission of a Si atom. $E_{before\ emission}$ is the energy of the system before emission of a Si atom. $E_{Si\ atom}$ is the energy of an atom in bulk Si.

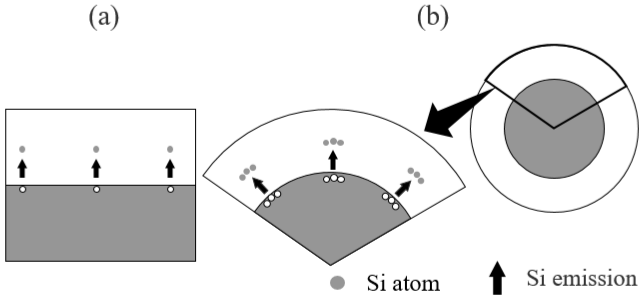

Fig.7: Schematic illustrations of the emission of Si atoms from the Si/SiO_2 interface. The black area is Si and the white area is SiO_2. (a) Si atom emission from a planar structure. (b) Si atom emission from a pillar structure. The geometry of the V-MOSFETs means that Si atoms are emitted more easily than in planar MOSFETs because the induced strain due to oxidation is larger.

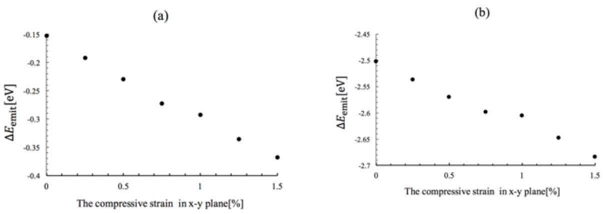

Fig.8: The dependence on strain of the energy change after the emission of Si atoms from (a) the $Si(100)/SiO_2$ interface and (b) the $Si(110)/SiO_2$ interface.

	strain	Si missing
dry oxidation	large	bad
wet oxidation	small	good
pyrogenic oxidation	small	good

Fig.9: Comparison between dry oxidation, wet oxidation and pyrogenic oxidation for the fabrication of V-MOSFETs.