Extended Abstracts of the 2017 International Conference on Solid State Devices and Materials, Sendai, 2017, pp573-574

M-1-01 (Invited)

CMOS Ising Computing for Combinatorial Optimization Problems

Masanao Yamaoka

Hitachi, Ltd.,

1-280, Higashi-koigakubo, Kokubunji-shi, Tokyo, 185-8601, Japan

Phone: +81-42-323-1111 E-mail: masanao.yamaoka.ns@hitachi.com

Abstract

A new computing using Ising model that is specialized to solve combinatorial optimization problems is proposed. The computing maps problems to an Ising model and solves the problems by its own convergence property. We fabricated prototypes of the computers and confirmed the power efficiency is 1800-times higher than that of the conventional von-Neumann computers.

1. Introduction

In the near future, the performance growth of von-Neumann computing will slow down due to the end of the semiconductor scaling. A natural computing, which maps problems to natural phenomena and solves the problems by its own convergence property, is proposed. The concept is indicated in Fig. 1. The natural computing does not use programs and does not solve problems step by step, and therefore, it does not expect the operation speed acquired by the semiconductor scaling. The quantum annealing machine[1] using superconductor is one of those computers and the neuro-morphic chip [2] is also one of them. As the other implementation, we proposed a CMOS Ising computing [3][4] to be specialized for solving combinatorial optimization problems.

2. CMOS Ising computing

The Ising computing maps the combinatorial optimization problems to Ising model, a model to express the behavior of magnetic spins, and solves the problems by ground-state search operations with its convergence property. The Ising model is shown in Fig. 2. The energy of the system is expressed as the formula besides the diagram. Here, σ_i is spin status, J_{ij} is interaction coefficient, and h_i is external magnetic field coefficient. In the CMOS Ising computing, the operation of the ground-state search of Ising model is mimicked by CMOS circuits as indicated in Fig. 3. Here, the spin values of +1 or -1 are stored in SRAM cells as "0" or "1". The interactions between spins are realized by memory cells and digital circuits, and are performed in parallel, and the necessary steps for the ground-state search are smaller than that using the conventional sequential computing, von-Neumann architecture.

3. CMOS annealing

For the ground-state search, we implement a CMOS annealing technique in CMOS Ising computer. In the CMOS annealing, the energy of Ising model is reduced along the line of energy landscape of the Ising model (solid arrows in Fig. 4). It is achieved by the digital circuits in the CMOS Ising computer. Only using the digital circuits, the state is trapped in the local minimum point of the energy landscape. To avoid trapping to local minimum points, we added random changes of the state (broken arrows in Fig. 4). In the CMOS Ising computing implementation, random numbers are injected and when the delivered number to the spin is "1" during interaction calculation, the calculated spin status is flipped [5].

4. Prototypes of Ising Computing

We fabricated prototype Ising chips with 65-nm process as shown in Fig. 5 [4]. In the Ising chip, 20 1k-spin sub-arrays are implemented and 20k spins are embedded. Fig. 6 shows the energy transition when the CMOS annealing is operated. As time goes, the energy is lowered. It means, the ground state search of CMOS Ising computing is correctly achieved. Fig. 7 shows the power efficiency compared to a conventional method, an approximation algorithm "SG3" run on a CPU when solving randomly generated MAX-cut problems. When the problem size is 20k spins, the energy efficiency is 1800 times higher than that of the conventional method.

We also implemented the CMOS Ising computing to FPGA chips as shown in Fig. 8. The FPGA is a reconfigurable device and we try to implement several Ising model structure. If helps the development of problem mapping techniques. The mapping technique is indispensable to use Ising computing for practical problems.

5. Conclusion

It is confirmed by prototype chip that the CMOS Ising computing can solve combinatorial optimization problems. The power efficiency is 1800-times higher than the conventional computing architectures. For the practical use, mapping technique of problems to the Ising model is indispensable.

References

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[5] M. Hayashi et. al., CANDAR 2015, pp. 542-546, 2015.
[6] C. Yoshimura et. al., CANDAR 2016, pp. 436-442, 2016.

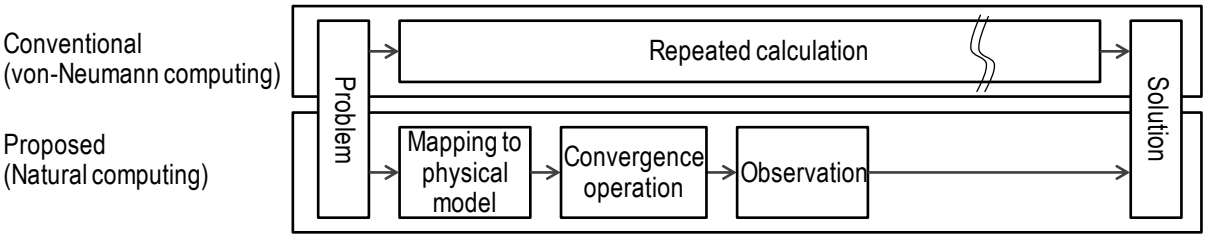

Fig. 1 Paradigm shift from von-Neumann computing to natural computing

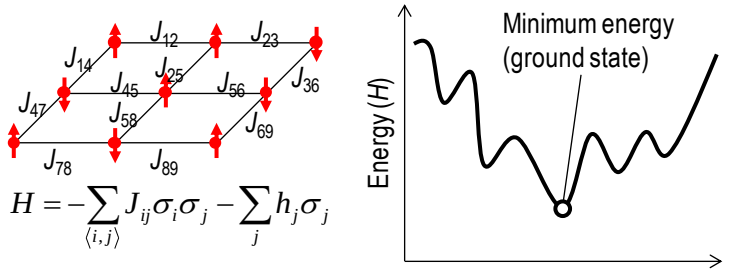

Fig. 2 Ising model and ground-state search using Ising model

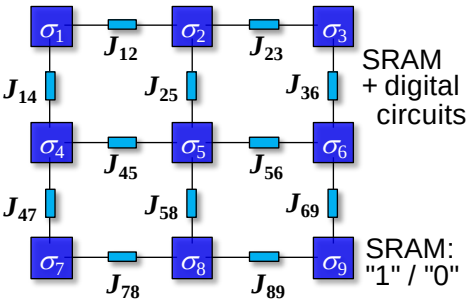

Fig. 3 Ising model mimicked by CMOS circuits, SRAM and digital circuits

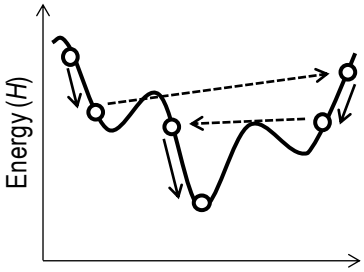

Fig. 4 CMOS annealing

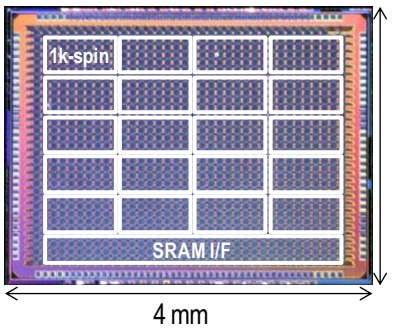

Fig. 5 Ising chip photograph

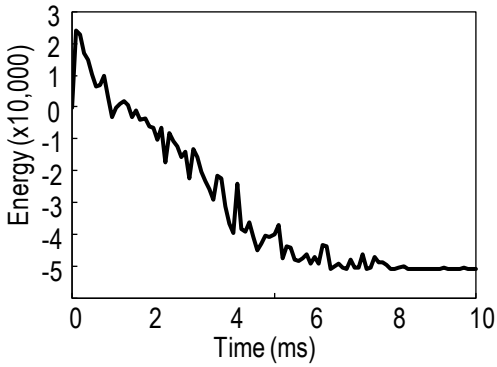

Fig. 6 Energy transition during operation of CMOS annealing

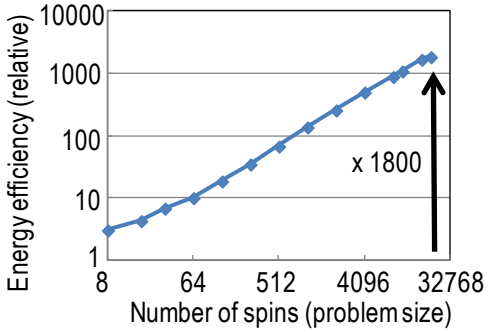

Fig. 7 Energy efficiency compared to an approximation algorithm running on CPUs

Fig. 8 FPGA prototype of CMOS Ising computer