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Grain Boundary Engineering of Solid-Phase Crystallized Ge on Glass by Controlling Atomic Density of Precursor

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Abstract

Polycrystalline Ge thin films are fabricated on glass by solid-phase crystallization. The control of the atomic density of the precursor enlarged the grain size and reduced the barrier height of the grain boundary. The hole mobility of the polycrystalline Ge reached 340 cm^2/Vs, the highest mobility of semiconductor films grown on insulator at low-temperature (< 900 °C).

1. Introduction

Germanium has been proposed as a major candidate for next-generation electronic devices because of its high carrier mobility and good compatibility with Si. In particular, the hole mobility of Ge is the highest among semiconductor materials, which can be used to realize high-performance complementary metal-oxide-semiconductor (CMOS) devices. The performance of the Ge-TFTs, however, has been no match for that of Si-MOSFETs. To further improve Ge-TFTs, one needs to study not only device technology but also crystallization techniques.

Polycrystalline Ge (poly-Ge) thin films have been directly formed on glass at low temperatures by using solid-phase crystallization (SPC) [1-3]. However, poly-Ge by this method consists of small grains, so further optimization of growth process is necessary. In this study, we focused on the atomic density of precursor for SPC.

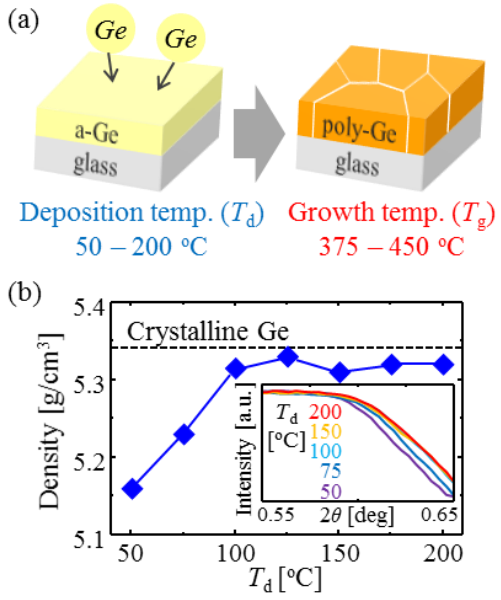

Fig. 1 (a) Schematic of sample preparation. (b) Density of amorphous Ge layers obtained from the inserted XRR patterns.

2. Experimental Procedures

As shown in Fig. 1(a), a 100-mm-thick Ge layer was deposited on SiO_2 glass substrates using the Knudsen cell of a molecular beam deposition system (base pressure: 5×10^{-7} Pa). The substrate temperature during the deposition, T_d, ranged from 50 to 200 °C. We note that T_d spontaneously rises from room temperature to 50 °C without heating the substrate because of the heat propagation from the Knudsen cell. The samples were then loaded into a conventional tube furnace in a N_2 atmosphere and annealed at 375 °C for 140 h, 400 °C for 20 h, and 450 °C for 5 h to induce SPC.

3. Results and Discussion

The as-deposited Ge layers were evaluated by X-ray reflectivity (XRR) and Raman spectroscopy. Fig. 1(b) shows that the density of the Ge layer approaches that of crystalline Ge with increasing T_d and becomes nearly saturated at T_d > 100 °C. Raman measurement revealed that the sample with T_d < 175 °C is amorphous and the sample with T_d = 200 °C includes both crystalline and amorphous states. The optical studies suggest the following: (i) higher T_d provides denser a-Ge; and (ii) the Ge layer begins to nucleate at T_d > 150 °C.

The grain size of the resulting poly-Ge layers was evaluated by electron backscattering diffraction (EBSD)

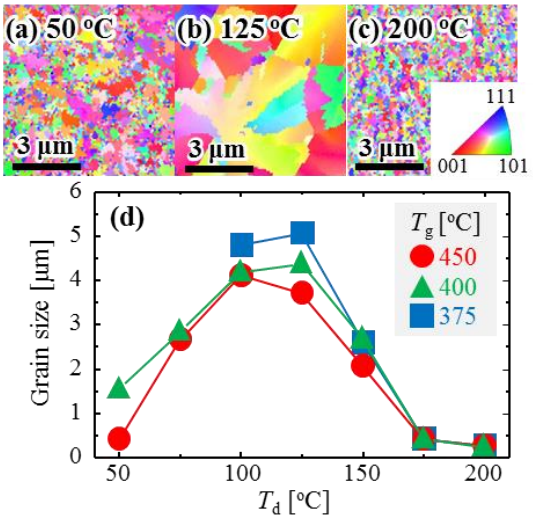

Fig. 2 (a)-(c) EBSD images of the samples where T_g = 450 °C. (d) T_d dependence of the grain size obtained from the EBSD analyses.

analyses. Figs. 2(a)-(c) show that the crystal orientation is almost random for all samples. EBSD images indicate that the sample with T_d = 125 °C exhibits grains that are one order of magnitude larger than those of the other samples. Fig. 2(d) shows that the grain size, as determined by the EBSD analyses, depends on both T_d and T_g. The grain size is a maximum at approximately T_d = 125 °C. The lower T_g provides a larger grain size, which agrees with the conventional SPC [1]. The samples with $T_d \leq 75$ °C annealing at 375 °C for 140 h were not crystallized, indicating that the higher T_d provides a higher growth rate.

The electrical properties of the resulting poly-Ge layers were evaluated by Hall measurements. All samples showed p-type conduction, like conventional non-doped poly-Ge [1-3]. This is because dangling bonds in Ge provide shallow acceptor levels and then generate holes at room temperature. Fig. 3 shows that the hole concentration depends on T_d and reaches a minimum at approximately T_d = 75–100 °C. The hole mobility is a maximum at T_d = 125 °C and increases with decreasing T_g. The sample with T_d = 125 °C and T_g = 375 °C exhibited the highest hole mobility, 340 cm^2/Vs. The hole mobility roughly increases with increasing grain size; however, there are exceptions. For example, the sample with T_d = 175 °C exhibited higher hole mobility than the sample with T_d = 75 °C (Fig. 3), whereas the grain size shows an opposing trend (Fig. 2). This behavior suggests that the hole mobility is not determined only by grain size, but also by some other factors.

According to the carrier conduction model in polycrystalline semiconductors proposed by Seto [4], the carrier mobility limited by grain boundary scattering can be determined using the following equation [4]:

$$\mu = \frac{Lq}{\sqrt{2\pi m^* kT}} \exp\left(-\frac{E_B}{kT}\right), \qquad (1)$$

where μ is the carrier mobility, E_B is the energy barrier height of the grain boundary, T is the absolute temperature, L is the grain size, m^* is the effective mass of carriers, and k is the Boltzmann constant, and q is the elementary charge. The T dependence of the hole mobility varied with T_d, indicating

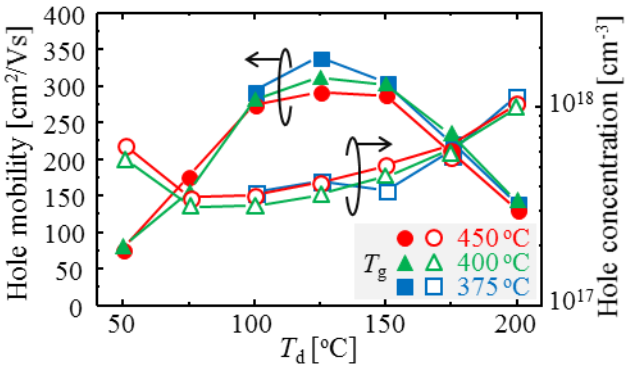

Fig. 3 Hole mobility and hole concentration for samples annealed at 375 °C, 400 °C, and 450 °C as a function of T_d.

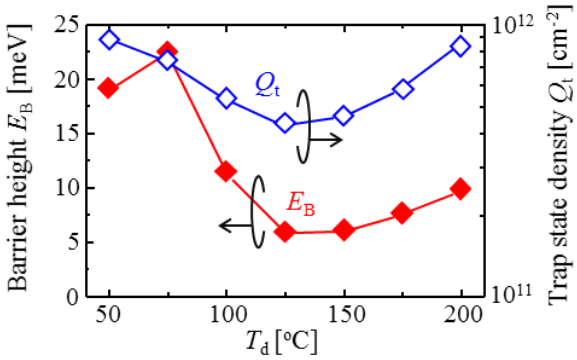

Fig. 4 Energy barrier height E_B and trap state density Q_t of grain boundaries for the samples with T_g = 450 °C as a function of T_d.

the difference in E_B. The Arrhenius plot of $\mu T^{1/2}$, exhibited downward-sloping straight lines for all samples. This behavior indicates that the carrier conduction in the poly-Ge layers is limited by grain boundary scattering. Fig. 4 shows that E_B, determined by the slopes of $\mu T^{1/2}$, depends on T_d. For T_d = 125 °C, E_B exhibits the minimum value, 6.4 meV. The trap state density Q_t in the grain boundary can be expressed using the following equation:

$$Q_t = \frac{\sqrt{8\varepsilon N E_B}}{q}, \qquad (2)$$

where N is the carrier concentration, ε is the dielectric permittivity [4]. Fig. 4 shows that Q_t depends on T_d. For T_d = 125 °C, Q_t exhibits the minimum value, 4.4 × 10^{11} cm^{-2}. The E_B and Q_t for T_d = 50 °C nearly agree with those of conventional poly-Ge [2]. These results indicate that the high hole mobility (340 cm^2/Vs for T_d = 125 °C) observed in this study is due to both the large grains and low Q_t.

4. Conclusion

The condition of the precursor for SPC dramatically influences the crystal quality and electrical properties in the resulting poly-Ge layer. The a-Ge precursor prepared at 125 °C led to a large-grained (5 μm) poly-Ge layer whose grain boundary exhibited a low energy barrier height (6.4 meV) because of the low trap state density (4.4 × 10^{11} cm^{-2}). This allowed for a hole mobility of 340 cm^2/Vs, the highest value among semiconductor layers formed on insulators at temperatures below 900 °C. The growth temperature was as low as 375 °C, allowing for Ge devices on plastic substrates. These results open up the possibility for developing advanced CMOS devices as well as system-in-displays and three-dimensional integrated circuits.

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