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MOCVD Selective Growth of InAs Nanowires on Patterned Silicon Substrate by Optimizing Gas Flow Rate and Annealing Temperature

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Abstract

Growth of periodically arranged heteroepitaxy of III-V nanowires (NWs) on lattice mismatched substrate is highly desirable. The quality of the oxide, NW growth temperature are significant parameters because it may enable seamless integration of NW-based electronic/optoelectronic devices. Here two sets of experiments were conducted to achieve good selectivity. Firstly, random InAs NW growth was grown on the Si(111) substrate covered with SiO_2 and then annealed in H_2 ambient at 850° C for different intervals. Secondly, Selective Area growth (SAG) of the InAs NW was performed at various indium molar flows. Through this approach, we determine the parameters namely annealing temperature, duration of annealing and amount of precursor which affect selectivity of NW nucleation on oxide substrate.

1. Introduction

Recent developments in synthesizing 1D compound semiconductor NWs on silicon substrate have been attracted for its potential of low cost. The unique properties of III-V compound semiconductors paved way for its achievements in wide range of device applications such as photonic devices, high speed electronics and energy harvesting devices. In particular, InAs NW is more a promising material because of its low effective mass, high electron mobility and saturation velocity. In addition to that, InAs fermi level pinning helps to make low electrical contact resistance [1]. To enable high SAG, the quality of oxide plays an essential role. The amount of indium molar flow and annealing temperature allow NW to nucleate on the oxide surfaces which ruins the process. Here we investigate the nucleation and growth of InAs NWs on patterned oxide silicon substrate as a result annealing the substrate at H_2 ambient using metal organic chemical vapor deposition (MOCVD) reactor. The SAG InAs NW morphology was characterized as a function of V/III precursor ratio and precursor flow rates.

2. Experiment

Synthesis of all InAs NWs were done by Veeco D180-MOCVD. Initially, Si(111) substrate (native oxide removed by using BOE) was covered by 20nm thick SiO_2 layer which was deposited by plasma enhanced chemical vapor deposition (PECVD) and the measured RMS value was 0.205nm. For first experiment, prior to loading the sample, substrate was dipped into diluted BOE for 20s and rinsed in DI water for 30s. The final thickness of oxide was around 14~15nm, which was measured using a SOPRA GES5 Ellipsometer. The removal of native oxides inside the holes is essential for later SAG process. After loading sample into chamber, the samples were annealed at 850°C in an H_2 ambient for 5 to 30 minutes, following that, the chamber temperature was reduced to 400°C for Silicon reconstruction with the ambient of $H2+AsH_3$. The sample was ramped to growth temperature 540°C. After the growth temperature was reached, both sources, trimethylindium (TMIn) and AsH_3, were introduced simultaneously. The TMIn and AsH_3 molar fractions were 1.85×10^{-5} and 8.12×10^{-4} respectively. For second experiment, the 20nm thick SiO_2 was patterned using E-beam and wet etching (diluted BOE) process. Following pattern development, 60s oxygen plasma cleaning and 20s diluted BOE etching were made to remove residue organic materials and native oxide inside the holes respectively. After loading the samples into chamber, annealing (5min) and growth steps were done similar to the first experiment, here AsH_3 was 8.12×10^{-4} and TMIn flow varied from 3.08×10^{-6} to 1.85×10^{-5}. The morphological and the detailed structural characteristics of the NW InAs NWs were observed by Scanning Electron Microscopy(SEM, Hitachi SU-8010) and Transmission Electron Microscopy (TEM, JEOL JEM-2010F, operated at 200 kV) respectively.

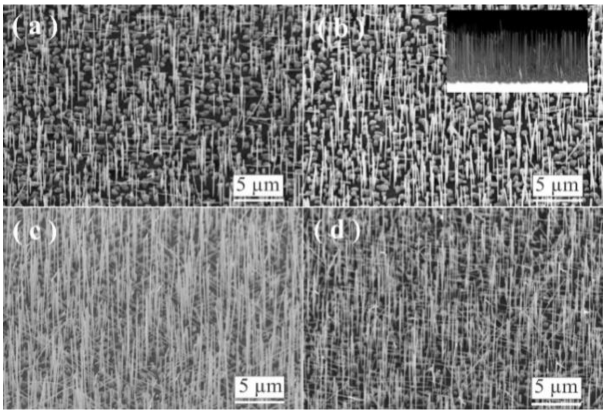

Fig. 1 Annealing of SiO_2/Si(111) with an H_2 ambient (a) 5 minutes, (b) 15 minutes, (c) 25 minutes(d) 30 minutes.

3. Results and Discussion

Fig. 1 displays the nucleation on SiO_2/Si(111) template after annealed at different time intervals. For 5mins annealing, the number of NW nucleation on the oxide is less, when the annealing time is increased, the oxide quality became worse, and hence NW nucleation density increase considerably. There are two reasons for the nucleation on oxide, first one, indium adatoms diffuse into oxide pin holes and start nucleation from the substrate [2] and second, the annealing duration may change the oxide into polycrystalline [3]. Comparing to Fig. 1 (a) and (b), Fig (c) and (d) have more inclined NWs because of polycrystalline orientation. Hence 5 mins annealing can reduce nucleation of NW on oxide. To prove Indium adatom diffusion, second set of experiments were performed with different TMIn flows for constant AsH_3 flow on patterned substrate. Here NWs were grown for 5 mins. Fig. 2(a) shows the indium scaling effect, when high indium composition flux reaches substrate, nucleation starts on patterned holes as well as on the oxide, and it became random NW growth. When the amount of Indium flow decreases, selectivity gradually increases and NW density on oxide decreases. From Fig. 2(b)-2(d), it is shown that NW nucleation on oxide is decreased. Hence, at lower indium flow rate, indium adatoms diffusion inside the oxide decreases and the maximum selectivity in patterned holes exists. For the NW morphology effect, when oxide started to suppress the nucleation, the amount of adatoms on the holes became larger. So it nucleates larger diameter NW at constant growth temperature of 540°C. By reducing the indium flow rate, NW diameter and height decreased. Fig. 3(a) shows the nucleation yield of NW for different age patterned sample. When the age increases, nucleation yield decreases. Because, the effective removal of oxide inside the holes became difficult. Fig. 3(b) shows high magnification image of Fig. 2(b) sample, where NW exhibits wurtzite (WZ) crystal structure with stacking fault. The insect FFT of Fig. 3(b) shows WZ signature of the NW. For resistivity measurement, p-doped Si samples with a 500nm SiO_2 (PECVD) insulating surface layer were prepared. Using photo lithography, Ni/Au (50/300nm) metal pad deposition was done by E-gun. On the above, NWs were mechanically transferred. Prior to making electrical connectivity between NW and metal pad using Focused Ion Beam (FIB), two sets of samples were prepared. One with HCL: H_2O (1:10) etch for 30s and another one is without etch. Fig. 3(c) shows the final device, here platinum was used as the interconnect metal which gives low energy barrier between NW and metal [4]. Fig. 3(d) shows that without wet etch treatment higher resistivity (49KΩ) was achieved compared to sample with wet etch (25KΩ) treatment. Wet etch helps to remove native oxide on InAs NW sidewall. Here the observed resistance of 25KΩ is dominated by stacking faults and mixed crystal structures in the NW [5].

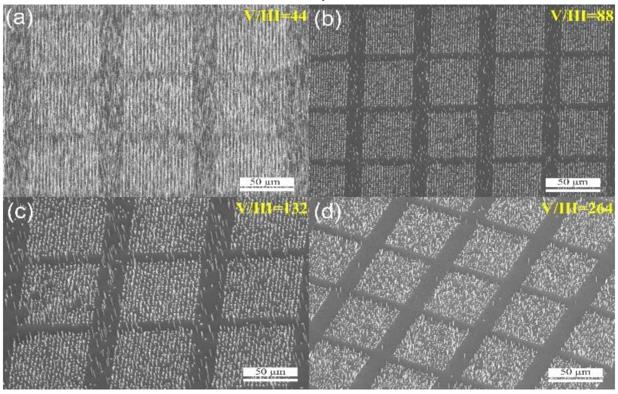

Fig. 2 Selectivity effect on Indium molar flow (a) V/III=44 (D~60nm), (b) V/III=88 (D~ 120-150nm), (c) V/III=132 (D~120nm), (d) V/III=264 (D~100nm).

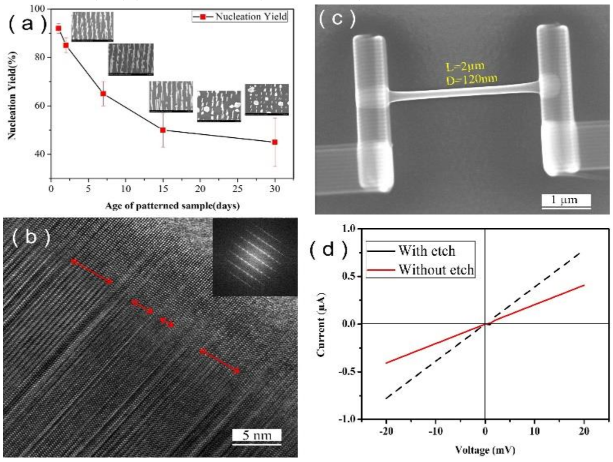

Fig. 3(a) NW Nucleation yield for different age of patterned sample, (b) TEM image of the NW for V/III=88 and insect shows WZ nature FFT of the NW, (c) Two-probe structure, (d) Two-Probe resistivity characteristics.

4. Conclusion

We investigate the factors that affect the MOCVD selective growth of InAs NW on patterned Silicon substrate. Reconstruction annealing duration and amount of indium flow play key roles to achieve maximum selectivity. We found that short annealing time and low indium precursors help to achieve maximum selectivity. Here WZ crystal structure was the dominant crystal structure than typical SAG-InAs mixed Zincblende/WZ structures for the InAs NW growth.

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References

[1]K. Tomioka, T. Tanaka, S. Hara, K. Hiruma, and T. Fukui, IEEE J. Sel. Top. Quantum Electron.**17** 1112 (2011).
[2]A.F.i. Morral, C. Colombo, G. Abstreiter, J. Arbiol, and J.R. Morante, Appl. Phys. Lett.**92** 063112 (2008).
[3]M.S. Carroll, L. Brewer, J.C. Verley, J. Banks, J.J. Sheng, W. Pan, and R. Dunn, Nanotechnology **18** 315707 (2007).
[4] B. Feng, S. Huang, J. Wang, D. Pan, J. Zhao, and H.Q. Xu, J. Appl. Phys.**119** 054304 (2016).
[5]C. Thelander, P. Caroff, S. Plissard, A.W. Dey, and K.A. Dick, Nano Lett.**11** 2424 (2011).