Extended Abstracts of the 2017 International Conference on Solid State Devices and Materials, Sendai, 2017, pp623-624

N-1-03

Etching Control in Side-Recess Formation of High Electron Mobility Transistor for High-Responsivity Terahertz Detector

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Abstract

A high-responsivity terahertz (THz) detector was fabricated using an InAlAs/InGaAs high-electron-mobility-transistor (HEMT) integrated with bow-tie antenna. For reduction in source resistance, we controlled side-recess spacing by measuring the source-drain current during the wet etching process. A maximum transconductance of 2.35 S/mm was obtained with 45-nm gate HEMT due to reduced source resistance, and a high current responsivity of 13 A/W was achieved at 280 GHz.

1. Introduction

The terahertz (THz) frequency range located between the lightwave and millimeter wave has been receiving considerable attention because of its many possible applications, such as imaging, spectroscopy, and high-capacity wireless communications [1]. Compact, high responsivity, and low noise detectors are key components for various applications of the THz waves. Recently, detectors using field effect transistors (FETs) have been studied intensively [2-5]. We proposed and fabricated a THz detector using an InGaAs composite-channel HEMT [6]. Conventional Schottky barrier diode (SBD) detectors have been used for various terahertz applications. However, current responsivity R_i decreases in high-frequency operation because the area of the Schottky junction is small, as required for increasing the cutoff frequency. In contrast with the SBD detector, the cutoff frequency of a HEMT detector can be increased by reduction in the gate length without reducing R_i. A high R_i (8 A/W) was achieved using a 50-nm gate-length HEMT with maximum transconductance $g_{m.max}$ of 1.6 S/mm [7]. Because, R_i is proportion to $g_{m.max}$, increase in $g_{m.max}$ by reduction in series resistance is effective for high responsivity.

In this study, we measured source-drain current during the wet-etching process for formation of side recess, and controlled the side-recess spacing. A short side-recess spacing of 150 nm was achieved. We obtained a high $g_{m.max}$ of 2.3 S/mm with 45-nm gate length due to reduced source resistance and high current responsivity of 13 A/W.

2. Experiments

The schematic device structure of our HEMT THz detector is shown in Fig. 1. An InP-based InAlAs/InGaAs composite-channel HEMT with two-finger T-shaped gates was integrated at the center of a bow-tie antenna. Although the HEMT is not operated the diode mode in this device, the HEMT still has diode-like characteristics in the I_d–V_{gs} characteristics. An irradiated THz wave can be detected by rectification. Using $g_{m.max}$ and subthreshold slope $S.S.$, R_i is roughly expressed as $R_i \approx g_{m.max} W R_a / S.S.$, where R_a is antenna impedance and W is gate width [6]. A high value of $g_{m.max}$ with small subthreshold characteristics is required for high responsivity.

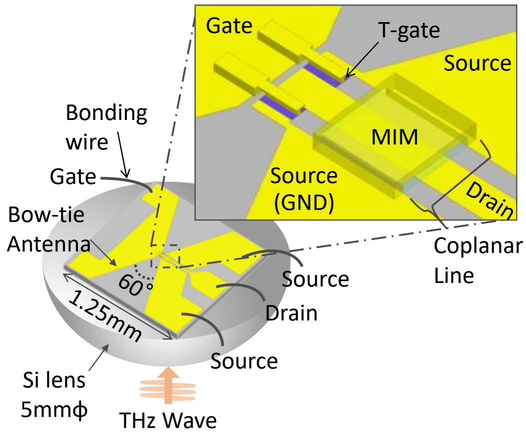

Fig. 1 Schematic of the HEMT THz detector structure integrated with bow-tie antenna.

The epitaxial layer structure was grown by molecular beam epitaxy on semi-insulating (100) InP substrates. From bottom to top, the layers consist of a 200-nm InAlAs buffer, a 10-nm InGaAs composite-channel, a 3-nm InAlAs spacer, a Si δ-doping of 5×10^{12} cm^{-2}, a 2-nm InAlAs barrier, a 3-nm InP etching-stopper, a 10-nm layer of n$^+$-InAlAs (3×10^{19} cm^{-3}), a 40 nm n$^+$-InGaAs contact layer (5×10^{19} cm^{-3}) , and a 9 nm high-indium-content n$^+$-InGaAs top contact layer (5×10^{19} cm^{-3}). We employed thick contact layer (from 15 nm to 40 nm) and high-indium-content n$^+$-InGaAs top contact layer for low contact resistance and sheet resistance. The 2-DEG mobility and density were 11200 cm/Vs and 3.61×10^{12} cm^{-2}, respectively, from Hall measurements at room temperature.

A tri-layer resist was used to form the T-shaped gate and a Pt-buried gate process was used to reduce the short channel effect. The fabrication process is briefly described as follows. First, the device was isolated by wet chemical etching ($H_2SO_4/H_2O_2/H_2O$) using a ma-N resist (Micro Resist Technology) mask. The source, drain, and antenna electrodes (Ti/Pd/Au) were formed by the standard lift-off process using a polymethyl methacrylate (PMMA) resist. The bow-tie angle was 60 deg. The HEMT surface was covered with a SiO_2 film as an etching mask for the formation of the gate recess structure. A tri-layer resist (ZEP/PMGI/ZEP) was coated onto the SiO_2 film. The top and bottom ZEP layers were separately exposed using 50-keV electron beam irradiation. The gate pattern was replicated on the SiO_2 film using CF_4 inductively coupled plasma reactive-ion etching (ICP-RIE), and the gate recess structure was formed by wet chemical etching. To reduce the source resistance, the wet etching control for short side-recess spacing is required. The details of gate recess formation is described in the next paragraph. Finally, a T-shaped gate electrode (Pt/Ti/Pt/Au) was deposited. The gate length was 45 nm.

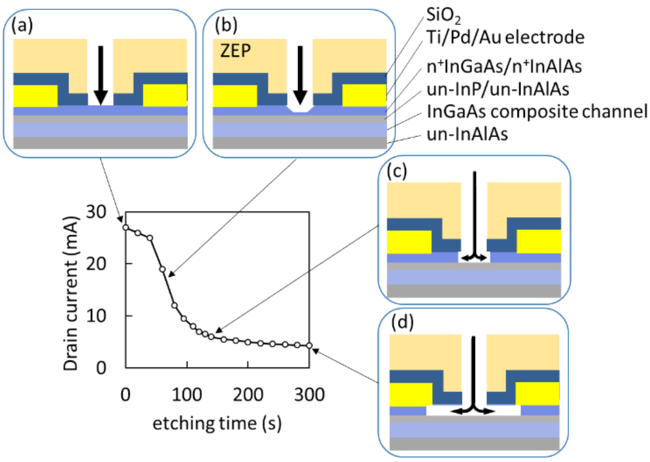

Fig. 2 Measured drain current as a function of etching time. Corresponding cross-sectional views for various etching times are also shown.

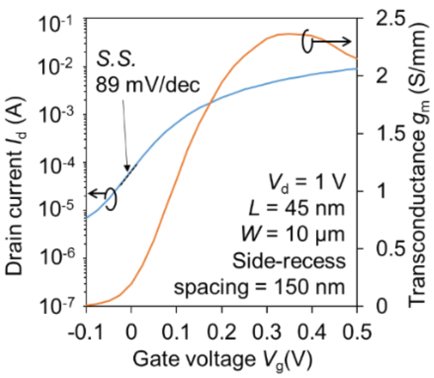

Fig. 3 I_d-V_{gs} and transconductance characteristics. Low subthreshold slope was obtained with Pt-buried gate.

In the gate recess formation, the drain current is measured during wet etching process. The measured drain current as a function of etching time is shown in Fig. 2. The source voltage is fixed at 1 V. First, the n^+InGaAs/n^+InAlAs contact layer, which has high conductivity, is etched by citric acid, and the current rapidly decreases. Corresponding cross-sectional view is shown in Fig. 2(a) and (b). Upon continued etching, the rate of current decrease becomes slow, because the contact layer is completely separated, and then the current flows the channel region, which has lower conductivity than the contact layer (Fig. 2(c) and (d)). The etching is stopped at (c) for short side recess spacing and reduction in the source resistance. A short side-recess spacing on one side of 150 nm was obtained in (c) case.

The measured I_d-V_{gs} and transconductace characteristics were shown in Fig. 3. We obtained high $g_{m.max}$ (2.35 S/mm) by the reduction in series resistance. The measured *S.S.* value was 89 mV/dec. The current responsivity R_i, measured as a function of the received power of 280 GHz signal, is shown in Fig. 4. The drain bias V_d was 0.5 V. The subthreshold voltage of 50 mV was applied to the gate. A maximum R_i of 13 A/W was obtained in the low-received-power region. The R_i drops with received power because of the degradation of nonlinearity in case of large signal. Higher R_i can be realized using a state-of-the-art HEMT having very high g_{mmax} of 3.1 S/mm [8].

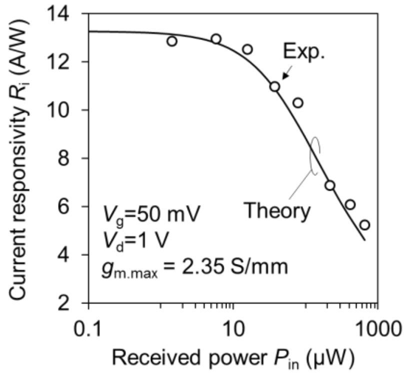

Fig. 4 Dependence of current responsivity R_i on received power P_{in}.

Acknowledgements

The authors thank Honorary Prof. Y. Suematsu and Emeritus Prof. K. Furuya of the Tokyo Institute of Technology for their continuous encouragement. We also thank Prof. S. Arai, Prof. Y. Miyamoto, Assoc. Prof. M. Watanabe, and Assoc. Prof. N. Nishiyama of the Tokyo Institute of Technology for fruitful discussions. This work was supported by the Grant-in-Aid (16H06292) from JSPS, CREST (JPMJCR1534) from JST, and SCOPE from MIC Japan.

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