Enhanced-Mode InAs QWFETs with the Source Connected Field Plate Technique for Low Power Logic Applications

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Abstract

In this work, we present the enhanced mode InAs QWFETs with the source field plate technique for low power logic applications. Excellent SS value of 64.1 mV/dec, DIBL value of 44 mV/V and a very high Ion/Ioff ratio of 2.4 × 10⁴ were achieved. Meanwhile, the OFF-state current and the leakage current were 51% and 64% suppressed, respectively, compared with the conventional InAs QWFETs.

1. Introduction

For post-CMOS, high electron mobility, III-V semiconductors have been the most promising materials for high performance and low power logic applications. The source connected field plate technique is used for AlGaN/GaN HEMTs to enhanced the power performance since this technique can not only smooth the electric field between the gate and drain but also reduce the leakage current. As the number of transistors in a microprocessor goes larger and larger, the leakage current issue becomes a much more severe problem for the low power logic application. Recently, many works of In₀.₅₃Ga₀.₄₇As based devices, like In₀.₅₃Ga₀.₄₇As QWMSFETs and MOSFETs, have been widely investigated for low power logic applications. However, the leakage issue and the Ion/Ioff ratio are still the Achilles’ heels of those reported lectures. It is little known that using the source connected field plate technique to improve the low power logic performance of the enhanced mode InAs quantum well field effect transistors (QWFETs). In this study, the enhanced mode InAs QWFETs with source connected field plate were studied to achieve excellent logic performance for low power logic applications.

2. Device fabrication and measurement

The layer structure includes highly Si-doped, In₀.₅₃Ga₀.₄₇As cap layers, an InP etch stop layer, an In₀.₅₂Al₀.₄₈As barrier layer, a Si planar doping layer, a thin In₀.₅₂Al₀.₄₈As spacer layer, and the In₀.₆₅Ga₀.₃₅As/InAs/In₀.₆₅Ga₀.₃₅As layers to improve the electron transport properties[3]. The device fabrication process includes mesa isolation, Ohmic metal deposition, silicon nitride passivation, gate recess, gate formation, and field plate structure. The device isolation was defined by wet etch using an H₃PO₄ base solution. Then, the non-alloy Ohmic metal (Ti/Pt/Au) was deposited and the source, drain spacing was 3μm. The T-shaped gate was achieved using E-beam lithography, and the Schottky gate metal (Pt/Ti/Pt/Au) was deposited. Finally, the source connected field plate was defined by E-beam lithography and the field plate metal (Ni/Au) was deposited by E-gun.

The electrical characteristics were measured by Agilent 4156C.

3. Results and discussions

Fig. 2 shows the output characteristics (IDS-VDS curves) of the source connected field plate (SCFP) enhanced mode InAs QWFET. The maximum drain current (IDS max) of the SCFP InAs QWFET was 272 mA/mm as the device drain voltage (VDS) and the gate voltage (VG) were both biased at 0.5 V. Fig. 3. shows the transfer characteristics (IDS VS. VG) of the SCFP InAs enhanced mode QWFET. The maximum transconductance (Gm max) of the device was 1202 mS/mm at VDS = 0.5V.

Fig. 4 compares the electrical characteristics (SS, Ion/Ioff ratio and the OFF-state current) of the enhanced mode InAs QWFETs with and without the SCFP at VDS = 0.5V. The excellent value of subthreshold slope (SS) of the SCFP device is 64.1 mV/dec which is close to the ideal value of MOSFETs. For the SCFP InAs enhanced mode QWFET, the Ion/Ioff ratio is a high value of 2.4×10⁴ which is higher than other In₀.₅₃Ga₀.₄₇As HEMTs owing to that the off-state current was effectively suppressed (51%) by the source connected field.
plate technique. With an SCFP technique, the $I_{\text{ON}}/I_{\text{OFF}}$ ratio was increased from $1.3 \times 10^4$ to $2.4 \times 10^4$. Meanwhile, the sub-threshold swing was also improved from 68.3 mV/dec to 64.1 mV/dec. The gate leakage was also reduced 64% (not shown here).

With a SCFP technique, the $I_{\text{ON}}/I_{\text{OFF}}$ ratio was increased from $1.3 \times 10^4$ to $2.4 \times 10^4$. Meanwhile, the sub-threshold swing was also improved from 68.3 mV/dec to 64.1 mV/dec. The gate leakage was also reduced 64% (not shown here).

![Image](image1.png)

**Fig. 2.** DC characteristics of the enhanced mode InAs QWFET with source field plate (Ids-Vds curves).

![Image](image2.png)

**Fig. 3.** Transfer characteristics of the enhanced mode InAs QWFET with source field plate at $V_{\text{DS}}=0.5\text{V}$ (Ids & Gm vs. Vgs).

![Image](image3.png)

**Fig. 4.** SS & $I_{\text{ON}}/I_{\text{OFF}}$ comparisons of the enhanced mode InAs with and without the source field plate technique at $V_{\text{DS}}=0.5\text{V}$.

4. Conclusions

In this study, the enhanced mode InAs QWFETs with the source-connected field-plate structure were studied. The OFF-state current was 51% suppressed, and the gate leakage was 64% reduced compared with the conventional InAs QWFET. The excellent logic performance of $SS = 64.1$ mV/dec, DIBL = 44 mV/V and a high $I_{\text{ON}}/I_{\text{OFF}}$ ratio of $2.4 \times 10^4$ were achieved. The results indicate that the enhanced mode InAs QWFETs with the source-connected field-plate is suitable for the low power logic applications.

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References