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Study of enhance mode π -gate InAs HEMT for logic application

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Abstract

In this study, an enhance mode (E-mode) π -gate InAs HEMT devices is presented for logic application. The foot of π -gate structure direct contact with buffer layer to improve the gate controllability and reduced off state leakage current. The π-gate device exhibits low subthreshold slope (SS) of 64 mV/decade, low off state leakage current is 5.5x10^{-3}mA/mm and high maximum current density of 450 mA/mm, at V_{DS}= 1 V.

1. Introduction

For device scaling in Si technology, the physical gate length of Si transistors is used in current 20 nm node generation and the size is expected to reach the limitation of 7 nm in 2018. Planar III-V compound semiconductor FET with Si technology is one of the promising solutions for the CMOS technology to extend Moore's law [1]. In general, III-V materials have approximately 50 to 100 times higher electron mobility than Si, and the extremely high transconductance demonstrated recently using InAlAs/InAs HEMTs on InP substrate with ultra-short gate length [2]. InAs possesses the properties of high electron mobility (20,000 cm^2/Vs) at room temperature, high electron peak velocity, low electron effective mass and a reasonable energy bandgap (~0.3 eV) in low operation bias. InAs has plenty of attractive advantages as the channel material of HEMTs for future high-speed and low-power logic applications [3]. The paper report 3-D fin structure can be used to improve gate controllability [4]. Besides, the low leakage current is the key issue for future VLSI technology. [5]

In this work, the 3-D π-gate structure is designed which directly contact with buffer layer for improving gate controllability and reduced off state leakage current. The device shows low subthreshold slope and decrease leakage current.

2. Device fabrication and measurement

In this work, the epitaxial layers of the HEMTs were grown on InP substrates by molecular beam epitaxy (MBE). The structure layers from bottom to top are composed of an InP semi-insulator substrate for better isolation between adjacent devices, an $In_{0.52}Al_{0.48}As$ buffer layer for better lattice match and 2DEG confinement. An InAs-based channel layer between two $In_{0.65}Ga_{0.35}As$ sub-channels are applied on the buffer to enhance the electron confinement and improve the electron transport properties. An InAlAs spacer layer is used to form heterostructure interface with channel. A Si δ-doped carrier supply layer in it to provide extra carriers. An InAlAs schottky layer to form schottky interface with gate metal. An InP etching stop layer is capable of controlling the depth of recess and providing a passivation surface of InAlAs layer. Finally, a highly Si-doped $In_xGa_{1-x}As$ cap layer is used to reduce the contact resistance. For the device fabrication, first, we used the phosphoric based solution to etch InGaAs cap layers, hydrochloric acid to etch the stop layer, and phosphoric based solution again to etch InAlAs/InGaAs layers. Then, the multilayer metal of Ti/Pt/Au was deposited by E-Gun evaporator forming ohmic contact. Subsequently, we used the inductively coupled plasma (ICP) etching with Cl_2 gas, hydrochloric acid etching the stop layer, and the inductively coupled plasma (ICP) etching with Cl_2 gas again to form 3-D π-gate structure. There are four 3-D π-gate structure on the 20um gate width device and the interval between each π-gate is 4 um. After that, the SiN_x film was grown by plasma enhanced chemical vapor deposition (PECVD) with process gases mixed with silane, ammonia, and nitrogen. The gate recess region was removed by anisotropic CF_4 inductive coupled plasma (ICP) dry etching. After dry etching, the cap layer etching performed by using PH-adjusted solution of succinic acid (S.A.) and H_2O_2. Then, Ti/Pt/Au (800/600/1800 Å) gate metal was evaporated by e-gun evaporation system, as shown in Fig.1.

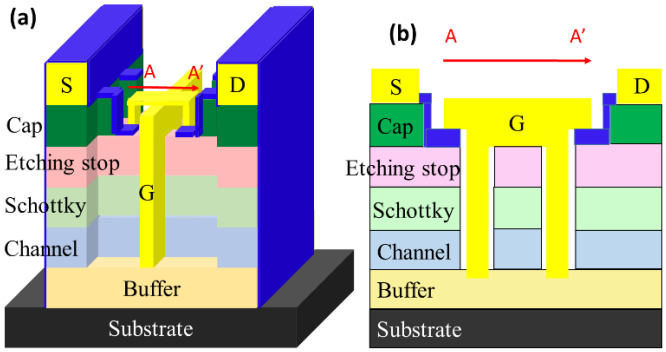


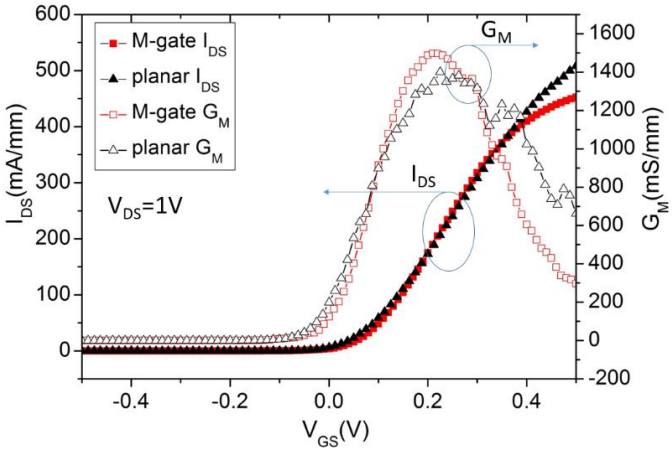
Figure 1. (a) Structure of the device in this study (b) A to A' cross section of the device

3. Results and discussions

In Fig2. shows I_D-V_G characteristic of the π-gate and planar device at V_{DS}= 1V. The π-gate devices presented the

transconductance Gm=1500mS/mm which is close to planar devices transconductance Gm=1400mS/mm. The drain current density of π-gate device is 452 mA/mm, and planar device is 508mA/mm. The 3-D structure etching reduces the cross-section area of channel, so drain current will slightly reduce. The threshold voltage from -0.01V to 0.02V. The reason for the device from D-mode to E-mode is the π-gate structure enhanced gate controllability. The foot of π-gate direct contact to the buffer layer, so the gate can control channel at the front and back side.

Fig3..shows the Subthreshold slope characteristics of π-gate and planar device at V_{DS}= 1V. The subthreshold slope (SS) of the π-gate is 64mV/decade compare to planar devices is 67mV/decade, which is close to the theoretical limit. The off state leakage current (I_{OFF}) from 82.95x10^{-3}mA/mm to 5.5x10^{-3}mA/mm. The π-gate reduced leakage current and improve the I_{ON}/I_{OFF} ratio from 6x10^3 to 8x10^4 as shown in Table I. Compared with other devices in the literature[6-15] the π-gate show excellent I_{ON}/I_{OFF} ratio and SS is show in Fig 4. .



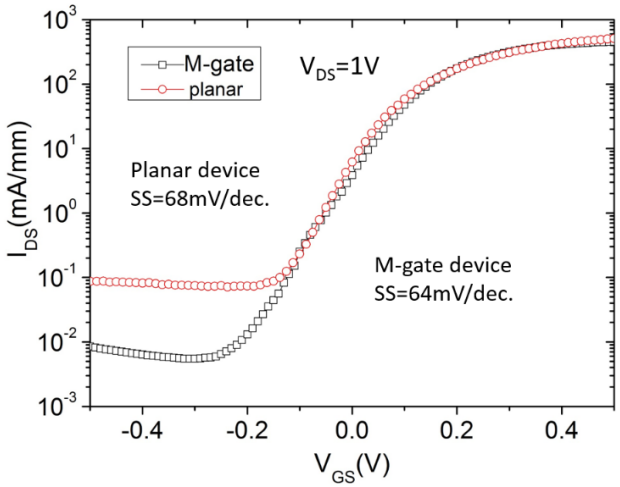


Figure 2. ID/Gm-VG characteristics of π-gate and planar device

Figure 3. Subthreshold slope characteristics of π-gate and planar device

4. Conclusions

In this work, E-mode InAs HEMT using π-gate structure have been fabricated. The foot of π-gate structure was designed to direct contact with buffer layer for improving the gate controllability and reducing off state leakage current. The π-gate device exhibit, low Subthreshold slope (64mV/decade) and low off state leakage current (5.5x10^{-3}mA/mm). The π-gate structure successfully improved the gate controllability, and shows the potential for future InAs HEMT logic application.

Table I. Compare DC characteristic for π-gate and planar devices

Gate structure	π-gate	planar
I_{DMAX}(mA/mm)	452	508
GM_{MAX}(mS/mm)	1500	1400
SS(mV/decade)	64	68
I_{OFF}(x10^{-3}mA/mm)	5.5	82.95
I_{on}/I_{off}	8x10^4	6x10^3
Vth(V)	0.02	-0.01

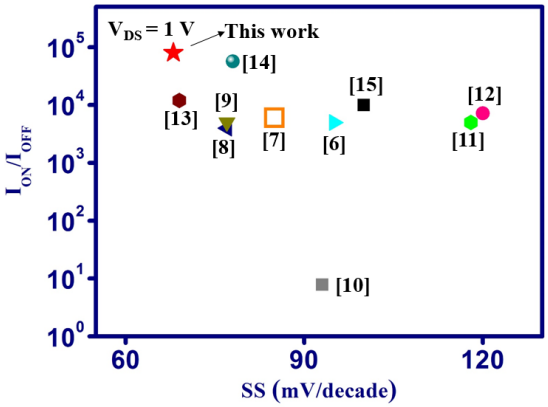


Figure 4. I_{ON}/I_{OFF} ratio as a function of SS for the π-gate and other device reported in the literature

Acknowledgements

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