Extended Abstracts of the 2017 International Conference on Solid State Devices and Materials, Sendai, 2017, pp651-652

N-3-05

Drain-induced barrier lowering in normally-off AlGaN-GaN MOSFETs with single- or double-recess overlapped gate

T. Sato[1*], K. Uryu[1], J. Okayasu[1], M. Kimishima[1], and T. Suzuki[2]

[1] *Advantest Laboratories Ltd.,*
48-2 Matsubara, Kami-Ayashi, Aoba-ku, Sendai, Miyagi 989-3124, Japan
*E-mail: taku.sato@advantest.com

[2] *Center for Nano Materials and Technology, Japan Advanced Institute of Science and Technology (JAIST)*
1-1 Asahidai, Nomi, Ishikawa 923-1292, Japan

Abstract – We investigated drain-induced barrier lowering (DIBL) in normally-off AlGaN-GaN metal-oxide-semiconductor field-effect transistors (MOSFETs) with a single- or a double-recess overlapped gate structure, in comparison with a conventional recess gate structure. The recess overlapped gate structures can suppress DIBL, where the double-recess is more advantageous for the DIBL suppression.

1 Introduction

AlGaN-GaN field-effect transistors (FETs) are attractive for use in high-power and high-frequency applications. While standard AlGaN-GaN FETs are normally-on devices, normally-off devices are highly desirable for switching applications. Several approaches have been reported for the normally-off operation [1–5]. Among them, AlGaN-GaN MOSFETs fabricated by deep gate recess etching through to the GaN channel [4] provide an excellent threshold voltage manufacturing stability. However, for short gate lengths and high drain voltages, the recess gate AlGaN-GaN MOSFETs often suffer from negative threshold voltage shifts owing to drain-induced barrier lowering (DIBL). In this work, we investigated DIBL in normally-off AlGaN-GaN MOSFETs with a single- or a double-recess overlapped gate structure, in comparison with a conventional recess gate structure.

2 Device fabrication

Figure 1 shows schematic cross sections of fabricated AlGaN-GaN MOSFETs with (a) a conventional recess gate structure as a reference (Ref.), (b) a single-recess overlapped gate structure (SRO) [5], and (c) a double-recess overlapped gate structure (DRO). For an n-GaN(5 nm)/$Al_{0.2}Ga_{0.8}$(22 nm)/GaN(2 μm) heterostructure grown by metal-organic chemical vapor deposition, device isolation was achieved by ion implantation. Ohmic recess with $\sim$ 10 nm depth was carried out by conventional dry etching using BCl_3/Cl_2 mixture gas. We also carried out gate recess as follows. For Ref. and SRO, as shown in Fig. 1 (a) and (b), a deep recess region (40 nm depth, 150 nm length) is formed. On the other hand, as shown in Fig. 1 (c), DRO has a shallow recess region (20 nm depth, 1.5 μm length) in addition to the deep recess region. As a gate dielectric, a 20-nm-thick Al_2O_3 film was deposited by atomic layer deposition using trimethylaluminum and oxygen plasma. Aluminum-based ohmic electrodes were formed on the ohmic recess region after Al_2O_3 film removal. Ni gate electrodes were formed on the Al_2O_3 gate insulator, as shown in Fig. 1 (a), (b), and (c).

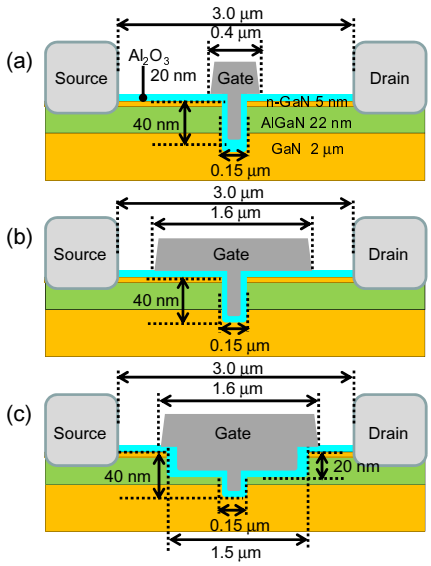

Fig. 1: Schematic cross sections of fabricated AlGaN-GaN MOSFETs with (a) Ref., (b) SRO, and (c) DRO.

3 Device characteristics

Figure 2 shows drain characteristics (drain current I_D vs. drain-source voltage V_{DS}) of AlGaN-GaN MOSFETs with (a) Ref., (b) SRO, and (c) DRO. On-resistances for Ref., SRO, and DRO are low, 3.3, 3.5, and 3.7 Ωmm, respectively. In addition, DRO exhibits low knee voltages and good I_D saturation in comparison with Ref. and SRO. Logarithmic-scale gate characteristics (drain current I_D vs. gate-source voltage V_{GS}) at V_{DS} = 15 V are shown in Fig. 3. We find that Ref. exhibits very poor sub-threshold characteristics, and also SRO exhibits poor one, both owing to DIBL. In contrast, for DRO, excellent sub-threshold characteristics is observed, indicating suppressed DIBL. Figure 4 shows linear-scale gate characteristics at V_{DS} = 1, 5, 10, and 15 V. Owing to DIBL, we observe negative threshold voltage shifts for Ref. and SRO, where the former exhibits more significant shifts. In contrast, for DRO, DIBL is suppressed; almost no shifts are observed. Figure 5 shows threshold voltages V_{TH} depending on V_{DS} for (a) Ref., (b) SRO, and (c) DRO. Significant DIBL for Ref. is confirmed in the range of V_{DS} = 1-15 V. We also find that DIBL occurs for SRO in the range of V_{DS} = 1-7 V, but is suppressed in the range of V_{DS} > 7 V. On the other hand, we can confirm no DIBL for DRO in the range of V_{DS} = 1-15 V. This implies that, both SRO and DRO can suppress DIBL, where DRO is more effective.

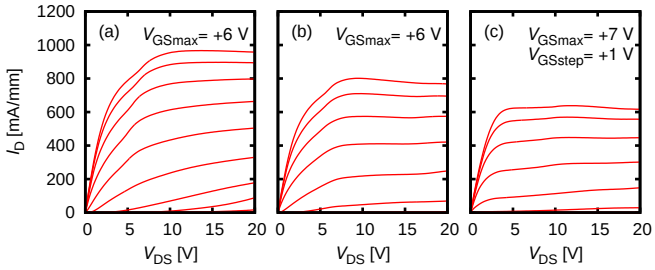

Fig. 2: Drain characteristics (I_D-V_{DS}) for (a) Ref., (b) SRO, and (c) DRO.

In order to elucidate the above results, we consider the potential V_X at the connection point between the local FET1 and FET2 in the DRO MOSFET shown in Fig. 6 (a), where FET1 with a local threshold voltage V_{TH1} corresponds to the deep recess gate region, and FET2 with a local V_{TH2} to the shallow recess overlapped gate region. Since $V_{TH1} > V_{TH2}$, the threshold voltage of the DRO MOSFET is dominated by FET1, $V_{TH} \sim V_{TH1}$. Let us consider the sub-threshold regime $V_{GS} \sim V_{TH} \sim V_{TH1}$, where FET1 is in the sub-threshold regime. For a high V_{DS}, due to current continuity, FET2 also must be in the sub-threshold regime $V_{GS} - V_X \sim V_{TH1} - V_X \sim V_{TH2}$; thus V_X is clamped at $\sim V_{TH1} - V_{TH2}$. On the other hand, for a low $V_{DS} < V_{TH1} - V_{TH2}$, since the FET2 cannot be in the sub-threshold regime, the effective drain voltage of the FET2, $V_{DS} - V_X$, should almost vanish due to current continuity; thus $V_X \sim V_{DS}$. For the SRO MOSFET, we can also consider the local FET1 and FET2 in the same way, where FET2 corresponds to the overlapped gate region without recess. As a result, V_X depends on V_{DS} as shown in Fig. 6 (b) for both DRO and SRO. For V_{DS} higher than the threshold voltage difference $V_{TH1} - V_{TH2}$, V_X clamped at $\sim V_{TH1} - V_{TH2}$ makes FET1 immune to DIBL, leading to the DIBL suppression in the DRO and SRO MOSFETs. We estimated the threshold voltage difference $V_{TH1} - V_{TH2} \sim 1$ V and ~ 7 V for DRO and SRO, respectively, being consistent with the DIBL behavior in Fig. 5; DRO and SRO can suppress DIBL, where the former is more advantageous.

4 Summary

We investigated DIBL in normally-off AlGaN-GaN MOSFETs with a single- or a double-recess overlapped gate, in comparison with a conventional recess gate. The recess overlapped gates can suppress DIBL, where the double-recess is more advantageous for the DIBL suppression. This is a consequence of a small threshold voltage difference between two local FETs corresponding to the deep recess gate and the shallow recess overlapped gate.

References

[1] M. A. Khan, Q. Chen, C. Sun, J. Yang, M. Blasingame, M. Shur, and H. Park, Appl. Phys. Lett. **68**, 514 (1996).

[2] X. Hu, G. Simin, J. Yang, M. A. Khan, R. Gaska, and M. Shur, Electron. Lett. **36**, 753 (2000).

[3] Y. Cai, Y. Zhou, K. J. Chen, and K. M. Lau, IEEE Electron Device Lett. **26**, 435 (2005).

[4] T. Oka and T. Nozawa, IEEE Electron Device Lett. **29**, 668 (2008).

[5] B. Lu, O. I. Saadat, and T. Palacios, IEEE Electron Device Lett. **31**, 990 (2010).

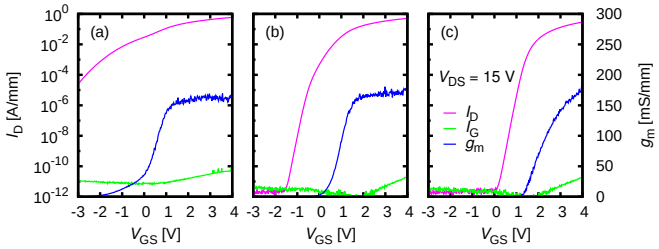

Fig. 3: Logarithmic-scale gate characteristics (I_D-V_{GS}) for (a) Ref., (b) SRO, and (c) DRO, at $V_{DS} = 15$ V and under a voltage sweep of $V_{GS} = +4 \rightarrow -3$ V. I_G: gate current, g_m: transconductance.

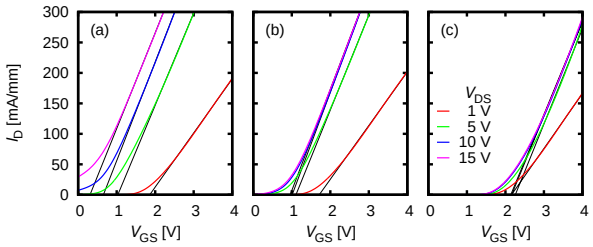

Fig. 4: Linear-scale gate characteristics (I_D-V_{GS}) for (a) Ref., (b) SRO, and (c) DRO, at $V_{DS} = 1, 5, 10$, and 15 V, and under a voltage sweep of $V_{GS} = +4 \rightarrow -3$ V.

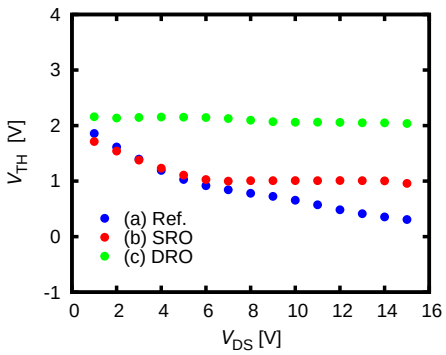

Fig. 5: V_{TH} depending on V_{DS} for (a) Ref., (b) SRO, and (c) DRO.

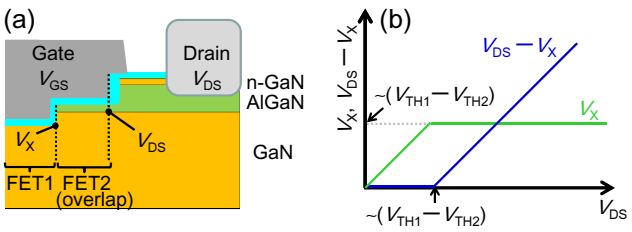

Fig. 6: (a) Schematic cross section of the DRO MOSFET with the local FET1 and FET2. (b) V_X and $V_{DS} - V_X$ in the sub-threshold regime, as functions of V_{DS}.