Extended Abstracts of the 2017 International Conference on Solid State Devices and Materials, Sendai, 2017, pp653-654

N-4-01 (Invited)

High Frequency GaN HEMTs for RF MMIC Applications

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Abstract

We report the first generation of GaN MMIC circuits that are based on the latest generation of (ft > 320 GHz and fmax > 580 GHz) GaN Transistors advanced under the DARPA Nitride Electronic NeXt-Generation Technology (NEXT) Program. These highly scaled GaN devices have 5 times higher breakdown voltage than transistors with similar high frequency RF power gain in other semiconductor systems (Si, SiGe, InP, GaAs).

1. Introduction

In this paper we report GaN MMICs that are based on the latest generation of (ft > 320 GHz and fmax > 580 GHz) GaN Transistors advanced under the DARPA Nitride Electronic NeXt-Generation Technology (NEXT) Program. Our device technology combines several unique features, including self-aligned gates, ohmic regrowth, and double-heterojunction vertically-scaled epitaxial structures which enable an unprecedented level of high-frequency performance [1-3].

Examples of the first generation MMIC's that are fabricated using these highly scaled devices include: Ka-band power amplifier (PA) having power added efficiency (PAE) of 59% measured at a frequency of 32 GHz, bias of 3 V and output power of 24.3 dBm, broadband Ka-band (27 GHz – 40 GHz) GaN LNA MMIC's having Noise Figure (NF) as low as 1 dB measured at a frequency of 37 GHz, NF < 2 dB with >24dB of gain across 28 GHz- 39.2 GHz frequency range, and a very broad range of usable DC bias conditions (Vd: 0.6V – 4V; Pdc: 5 mW- 310 mW.) The measured PAE of reported Ka-band MMIC PA, represent a significant improvement in PAE over values reported for other semiconductor technologies at this frequency band as well as for Ka-band GaN MMICs built in lower frequency GaN nodes. The measured NF of Ka-band LNA represents the lowest NF reported for GaN MMIC in this frequency range and compares favorably to the best values reported for the best competing semiconductor technologies.

2. Ka-Band MMIC PA

We designed and built high efficiency Ka-band MMIC PA in and Ka-band MMIC LNA in T4-A GaN process to illustrate the performance improvements that can be achieved with higher frequency GaN devices by taking advantage of high device gain at the higher order harmonics to achieve high efficiency switching mode waveforms at device output. The single stage Ka-band PA MMIC was realized in 50 um thickness microstrip topology by power combining four 4x37.5 μm unit cells. Figure 1 shows micrograph of the MMIC,

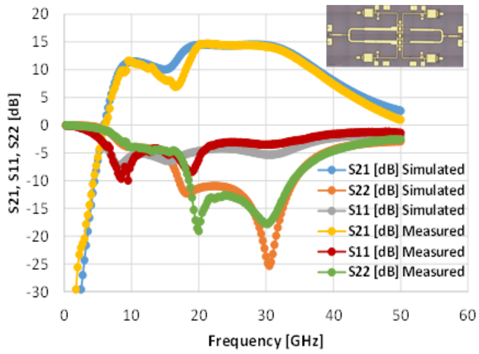

Fig. 1 Micrograph of 4x4x37.5 μm Ka-band GaN MMIC (top plot inset), Small Signal S-parameters measured and simulated at Vds = 3V.

measured and simulated small signal gain, and simulated current and voltage waveforms at the drain reference plane of one of 4x37.5 μm building blocks of this high efficiency MMIC PA.

Fig. 2 shows Pin/Pout power sweeps measured at a frequency of 32 GHz and a quiescent drain voltage of 2 V and 3 V respectively, and power vs frequency performance of the MMIC at drain bias of 2 V and Pin of 13 dBm. The quiescent drain current was adjusted for highest peak PAE performance, hence, gain expansion in Pin/Pout curves. The measured peak PAE of a MMIC was 59% for both drain bias biases with associated Pout of 21.2 dBm and 24.3 dBm, and associated gain of 8.9 dB and 8.2 dB, respectively, for quiescent bias of 2 V and 3 V. The measured peak drain efficiency of a MMIC was 71% and 69%, respectively, at drain bias of 2 V and 3 V. After accounting for 0.3 dB insertion loss of the output combining network the estimated drain efficiency of the device was 75% and 73%, respectively, for drain bias of 2 and 3 V.

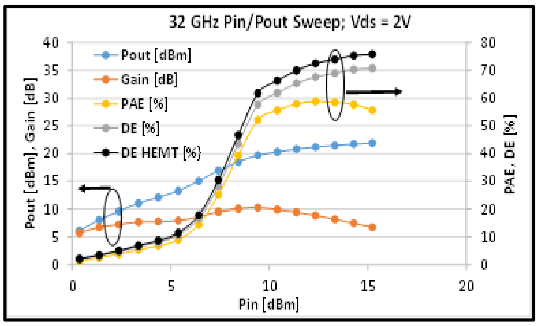

Fig. 2 Power-in Power-out characteristics of 4x4x37.5 um GaN MMIC PA from measured at a frequency of 32 GHz and quiescent drain bias voltage of 2 V.

3. Ka-band GaN MMIC LNA

Small signal noise models and non-linear large signal device models used for GaN MMIC design were extracted from

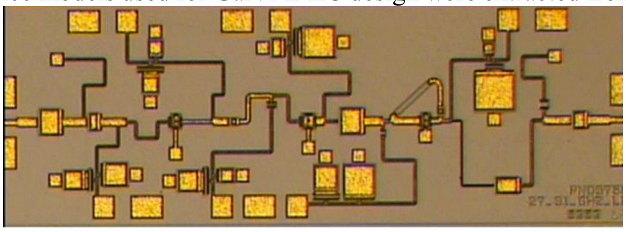

Fig. 3 Photograph of the Ka-band LNA designed using T4-A technology.

measured characteristics of the first generation T4-A devices. The LNA design goal was to optimize MMIC performance for the lowest attainable noise figure and good return loss across the 27 GHz- 40 GHz frequency range. We selected a 4x20 μm gate width transistor (80 μm total gate width) as the building element because it yielded the optimum combination of noise match and return loss.

Figure 4 shows small signal S-parameters of the Ka-band LNA measured on wafer at a drain bias of 2 V and drain current of 41 mA. The LNA has flat gain of 25 dB ± 2 dB over the desired 27 GHz – 40 GHz frequency range (27 dB peak gain at 27 GHz with < 0.3 dB/GHz gain slope over the 27 - 40 GHz frequency range). Data in Fig. 4 show that the MMIC is well matched into a 50 ohm system.

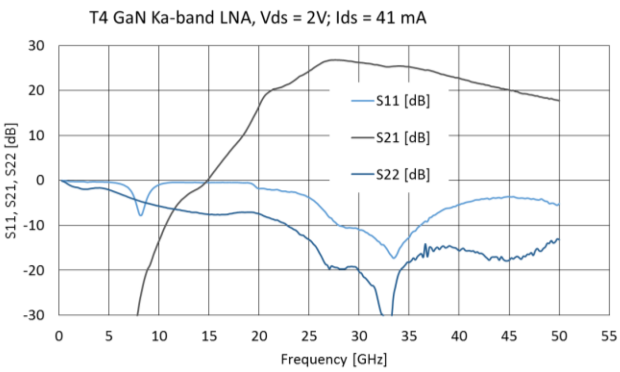

Fig. 4 Small signal response of the T4-A Ka-band GaN MMIC LNA measured on wafer at Vds = 2 V, Ids = 41 mA.

The noise figure of the LNA was measured on wafer over 26.5 GHz to 39.2 GHz frequency range for DC bias conditions ranging from Vds = 0.5 V; Ids = 10 mA (5 mW DC bias consumption) up to Vds = 3 V; Ids = 41 mA (124 mW DC bias consumption). Noise figure characterization was performed at room temperature (20 □C). Fig. 6 shows the measured Noise Figure and Associated Power Gain of the LNA at different bias conditions. Each trace corresponds to a different DC bias condition as indicated in by the legend.

The LNA has an average NF of 1.33 dB across 30 - 39.2 GHz frequency band measured for DC biases exceeding 83 mW (Vds = 2V, Ids = 41.5 mA). Under these bias conditions the LNA has a minimum NF of 1 dB measured at a frequency of 37 GHz. The LNA gain extracted from NF measurements is in excellent agreement with gain measured by small signal S-parameters. Our reported data represent, to the best of our knowledge, the lowest NF reported to date for a GaN MMIC LNA in this frequency band. Data shown in Fig. 5 also illustrate that this LNA maintains excellent NF characteristics over the entire DC bias range. The average NF of 2.1 dB, measured at extremely low DC bias of 5 mW, is near the state-of-the-art for low power MMICs operating in the 30-39.2 GHz frequency range

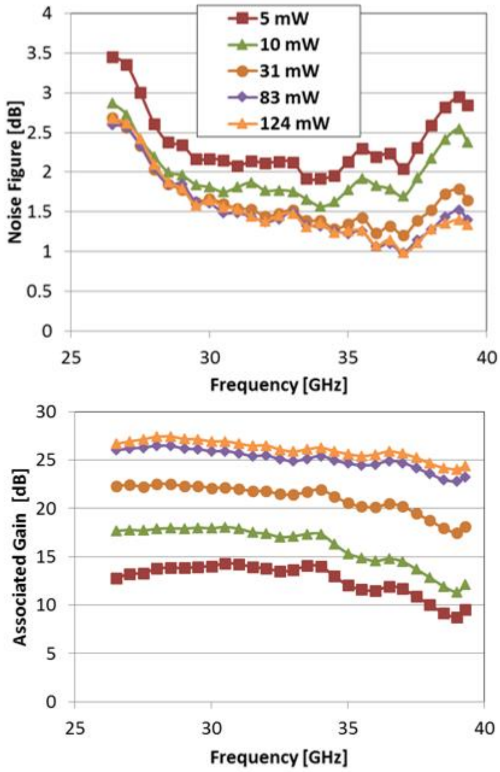

Fig. 5 MMIC LNA Noise Figure (top) and Gain (bottom) measured on wafer. Each trace corresponds to DC bias condition as indicated in a legend.

Acknowledgements

This work was sponsored by the Defense Advanced Research Projects Agency (DARPA) Nitride Electronic NeXt-Generation Technology (NEXT) program under Contract No. HR0011-09-C-0126, program manager Dr. Daniel Green, COR Dr. James Gillespie Air Force Research Laboratory. The views and conclusions contained in this document are those of the authors and should not be interpreted as representing the official policies, either expressly or implied, of the Defense Advanced Research Projects Agency or the U.S. Government.

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