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High Performance Tri-Gate AlGaN/GaN Power HEMTs

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Abstract

High performance AlGaN/GaN high electron mobility transistors (HEMTs) on silicon substrate was demonstrated based on tri-gate topology. The issue of short channel effect (SCE) was resolved by applying tri-gate architecture. The optimized tri-gate structure reduced the OFF-state current (I_{OFF}), subthreshold swing (SS) and further enhanced the ON/OFF ratio. The device with W_{fin} of 2µm exhibits low SS of 65 mV/decade, low I_{OFF} of 7nA/mm, and ON/OFF ratio up to 8 orders, showing full potential for future power applications.

1. Introduction

AlGaN/GaN high-electron-mobility transistors have emerged as promising devices for high speed and high power applications due to impressive characteristics such as high breakdown voltage, high current densities and high saturation velocity [1]. The gate length (L_g) of transistors is usually scaled down to operate at higher speed. However, when the Lg is shortened, the short-channel effect (SCE) becomes inevitable, showing increased subthreshold swing (SS) and I_{OFF} [2]. Therefore, the 3-D tri-gate architecture is derived. When compared with conventional planar transistors The extra sidewall gates offer additional electrostatic control which reduces both the I_{OFF} and SS [3].

In this work we present AlGaN/GaN tri-gate power HEMTs on silicon showing low subthreshold swing (SS) of 65 mV/decade, which is close to the theoretical limit and a large ON/OFF ratio of 10^8. The implement of 3D tri-gate topology enables better gate controllability, which not only improves the ON/OFF performance but also results in positive shift of threshold voltage (V_{th}) [4].

2. Device fabrication and measurement

The AlGaN/GaN structure was grown by MOCVD on silicon substrate consisting 1 µm GaN buffer, 22 nm undoped AlGaN barrier and 3 nm undoped GaN cap layer. The device fabrication started with ohmic contact formation. Multilayer metal consisting Ti/Al/Ni/Au was deposited using E-Gun evaporator and was then annealed by rapid thermal annealing (RTA) system at 850°C (30 sec) in N_2 ambient. Device isolation was executed using Cl_2-based inductively coupled plasma (ICP). The etching depth of the isolated area was 200nm. Then, 8 nanowires with fin width (W_{fin}) of 2µm and height of 200 nm was defined using electron-beam lithography and ICP. RTA process in N_2 ambient was used for surface recovery after the fin etching for better surface morphology. The distance between two adjacent fin structure is 500nm. Finally, the 400nm gate region was defined by electron-beam lithography and Ni/Au gate metal was deposited by E-Gun evaporator, the structure of the device is shown in Fig. 1. AlGaN/GaN HEMTs with planar structure was also fabricated on the same chip for reference. Device characteristics were normalized by the width of device (20 µm) in both planar and tri-gate devices and Agilent E5270B power device analyzer was used for DC characteristic measurement.

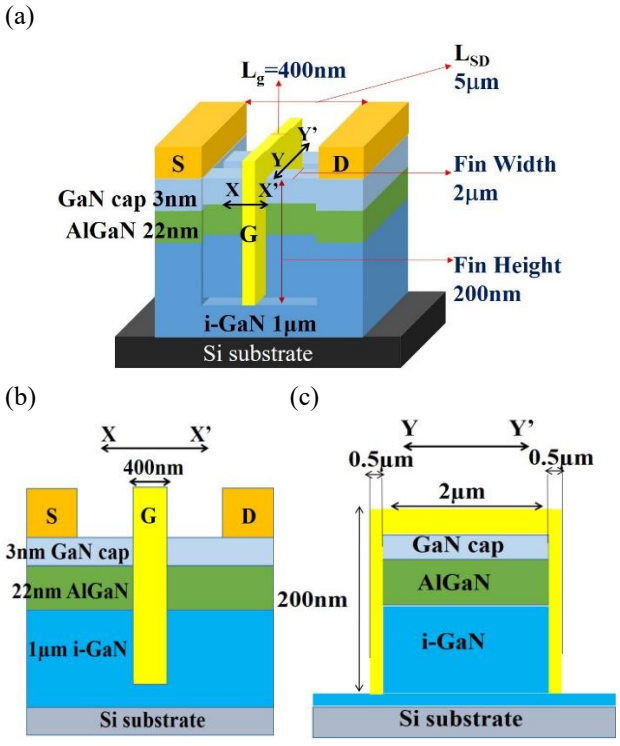


Fig. 1. (a) Schematic illustration of AlGaN/GaN tri-gate HEMT structure. (b) Front view (c) Side view

3. Results and discussions

Fig. 2 shows the subthreshold characteristics of both the tri-gate and planar device. The SS of the tri-gate device is descended from 144 to 65 mv/decade, which is close to the theoretical limit. The reason for the excellent SS measured is

mainly due to the enhanced gate controllability of the tri-gate structure, which further eliminates the effect of depletion capacitance under the conduction channel [4]. The off state leakage current (I_{OFF}) is reduced from 0.23μA to 7nA/mm. Therefore, the ON/OFF ratio is elevated from 10^6 to 10^8 due to the suppressed I_{OFF}.

Fig. 3(a) shows I_D-V_G characteristics of the devices. The planar and tri-gate devices presented transconductance (g_m) of 157 and 143 mS/mm and a positive shift of threshold voltage from -4.5V to -3V is observed. This phenomenon is mainly due to strain relaxation of the AlGaN/GaN tri-gate structure [5].

In Fig. 3(b), degraded on-resistance (R_{ON}) and drain current (I_D) is observed due to partial removal of the two-dimensional electron gas (2DEG) when etching nanowires with the ICP system [6]. However, it can be seen as a trade-off for the remarkable progress of the improved SS, ON/OFF ratio and the off state leakage current. Table I. shows the comparison of DC characteristics for the planar and tri-gate device. On the other hand, Table II. displays comparison of ON/OFF ratio and SS with other tri-gate GaN devices.

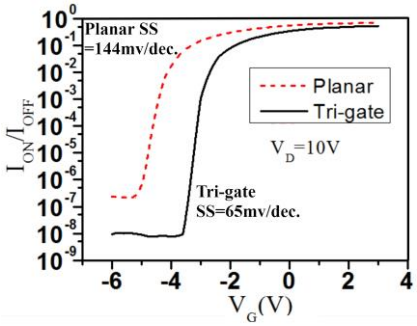
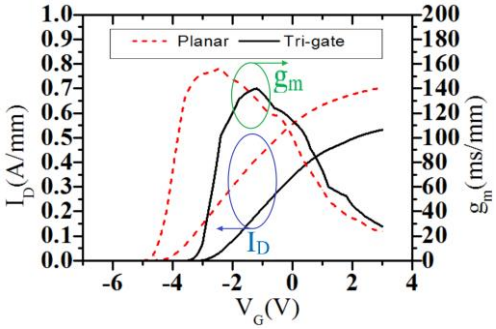


Fig. 2 Subthreshold Swing characteristics of planar and tri-gate HEMTs.

(a)



(b)

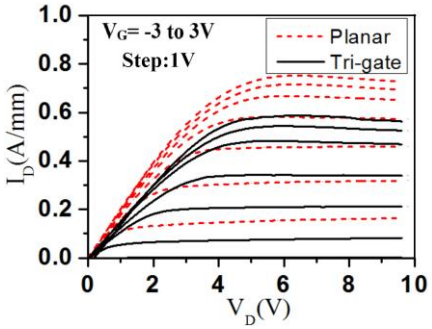


Fig. 3. (a) I_D-V_G, (b) I_D-V_D characteristics of planar and tri-gate HEMTs.

Gate Structure	Planar	Tri-gate
I_{DMAX}(mA/mm)	752	587
G_{MMAX}(mS/mm)	157	143
V_{th}(V)	-4.5	-3
R_{ON} (Ω·mm)	4.66	6.24
SS(mV/decade)	144	65
I_{ON}/I_{OFF}	3.2×10^6	10^8

Table I. Comparison of DC characteristics for planar and tri-gate HEMTs.

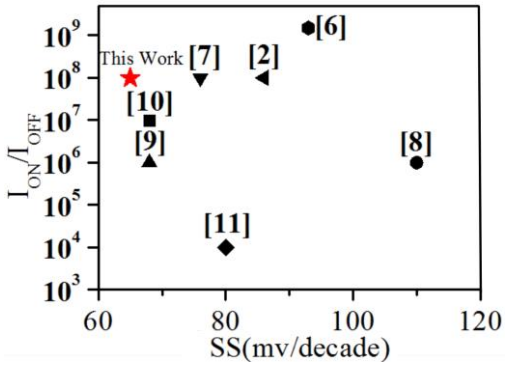


Table II. Comparison of ON/OFF ratio and SS with other tri-gate GaN devices [2], [6], [7] and [8] – [11].

4. Conclusions

In this work, high performance tri-gate AlGaN/GaN power HEMTs on silicon have been fabricated. The device exhibits low gate leakage current (7nA/mm), low SS (65mV/decade) and ON/OFF ratio up to 8 orders. The tri-gate architecture successfully improved the SS and I_{OFF} with an enhanced ON/OFF ratio, demonstrating great potential for future power application.

Acknowledgements

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