Extended Abstracts of the 2017 International Conference on Solid State Devices and Materials, Sendai, 2017, pp657-658

N-4-03

Back-gate effect on p-channel GaN MOSFETs on Polarization-Junction Substrate

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Abstract

GaN-based p-channel devices using two-dimensional hole gas (2DHG) are desirable to realize GaN CMOS circuits. Threshold voltage control using the two-dimensional electron gas (2DEG) potential as a back-gate is useful for the circuit design. In this paper, the back-gate effect on p-channel GaN MOSFETs on the polarization-junction (PJ) substrate is studied. The obtained dependence of threshold voltage on back-gate voltage is almost twice larger than the value expected from the device structure.

1. Introduction

GaN-based n-channel devices using two-dimensional electron gas (2DEG), *i.e.* high electron mobility transistors, are promising candidates to realize next-generation monolithic power integrated circuits. Due to the superior material properties, GaN devices show ultra-low on-resistance, high breakdown voltage, high switching capability, and wide range temperature operations [1-3]. On the other hand, GaN-based p-channel devices using two-dimensional hole gas (2DHG) are desirable to realize CMOS circuits and has been demonstrated [4, 5]. Owing to the nature of polarization-induced carriers, 2DEG and 2DHG densities are temperature independent [6]. In conjunction with the material stability of GaN, GaN CMOS technologies are promising candidates for applications for hash environment. Recently, CMOS operation using p-GaN [7] and 2DHG [8] has been demonstrated. However, the number of reports on p-channel GaN devices is still not much, and the evaluation of the electrical properties has not been enough. Moreover, the p-channel MOSFETs using 2DHG on polarization-junction (PJ) substrates were found to act as back-gate MOSFETs [8]. In this paper, the back-gate effect on p-channel GaN MOSFETs on the PJ substrate is evaluated, and the high sensitivity of threshold-voltage to the back-gate voltage is discussed.

2. Device fabrication

Fig. 1(a) shows schematic structure of a PJ wafer, where hole and electron are generated by polarization charges without impurity doping. In this study, the PJ was constructed with an undoped GaN/$Al_{0.23}Ga_{0.77}N$/GaN double heterostructure grown on a sapphire substrate. The 30-nm-thick top p-GaN layer enables formation of ohmic contacts to the 2DHG. P-channel MOSFETs' structure is shown in Fig. 1(b). An ohmic contact to the 2DEG was employed as the back-gate electrode, and the 2DEG potential can be controlled by the voltage applied to the back-gate electrode (V_{bs}).

The mesa structures illustrated in Fig. 1 (b) were formed by ICP etching. Under the MOS gate, a 17-nm-thick undoped GaN layer remains on the AlGaN layer. After a 15-nm-thick SiO_2 was deposited using atomic layer deposition (ALD) as the gate insulator, metal electrodes were formed by lift-off processes. The electrodes to the 2DEG were formed using Ti/Al/TiN on the etched AlGaN surface and annealed under N_2 ambient at 900 °C. Then, the electrodes to the 2DHG were formed using Ni/Au and annealed at 500 °C in N_2 + O_2 (5%) atmosphere. Finally, the gate electrodes composed of W/TiN were deposited on the gate insulator. The source-drain distance and gate length was designed at 80 μm and 60 μm, respectively.

3. Result and discussion

All measurements in this study were performed at room temperature. Fig. 2(a)-(c) shows I_d–V_{ds} characteristic of the fabricated device under the V_{bs} of 0, 4, and 6 V, respectively. These I_d–V_{ds} characteristics are similar to those of fully depleted silicon-on-insulator (FDSOI) MOSFETs. To evaluate the back-gate effect on the device characteristics, I_d-V_{gs} characteristics were measured under the V_{bs} ranging from 0 to 10 V, as shown in Fig. 3(a). It was found that threshold voltage (V_{th}) decreased as the V_{bs} increases. On the other hand, the I_d-V_{gs} curves with small V_{bs} showed large off current in the range of the V_{gs} below V_{th}, that is known as the back-channel current for FDSOI MOSFETs. Figure 3(b) shows log-scale I_d-V_{gs} characteristics. As decreasing the back-channel current, on/off ratio improved up to the V_{bs} of 2 V. Above the V_{bs} of 2 V, the gate leakage current became dominant of the total current in the device, that results in making the evaluation of off-state difficult. On the other hand, because I_d is enough larger than gate and back-gate current under the on-state with moderate gate voltage, the V_{th} dependence on V_{bs} can be discussed. Fig 3(c) shows the V_{th} dependence on V_{bs}. Here, the V_{th} was evaluated as the V_{gs} axis intercept of the linear extrapolation of the $I_d^{0.5}$-V_{gs} characteristics. In the range of V_{bs} from 0 to 5 V, V_{th} shows

linear correlation with the V_{bs} with the slope of -1.15. The slope of the V_{th}-V_{bs} characteristics is known for the back-channel depletion region of full-depletion type devices to be described as

$$\frac{\partial V_{th}}{\partial V_{bs}} = -\frac{C_{BG} \cdot C_S}{C_{FG}(C_{BG} + C_S)} \qquad (1),$$

where C_{FG}, C_S, and C_{BG} corresponds to the front-gate capacitance, semiconductor-layer capacitance, and back-gate capacitance, respectively. Regarding the dielectric constant of SiO_2, GaN, and $Al_{0.23}Ga_{0.77}N$ as 3.9, 9.5, and 9.27, respectively, and applying each designed thickness 15, 17, and 48 nm, respectively, the value of Eq. (1) should be -0.55, which means the V_{th} sensitivity to V_{bs} of the evaluated devices is almost twice larger than the model of full-depletion type back-gate devices. The origin of this high sensitivity has not been clarified yet, while it might be attributed to the internal electric field distribution and resulting change in the front-channel surface potential.

4. Conclusions

2DHG p-channel GaN MOSFETs with a back-gate using 2DEG potential were fabricated on a PJ substrate, and the back-gate effect on the threshold voltage of p-channel MOSFETs was evaluated. As a result, the sensitivity factor of V_{th} to V_{bs} was found to be -1.15, which is almost twice larger than the value expected from the device structure. The author believes that such larger V_{th}-controllability is preferable for the design of GaN devices and circuits.

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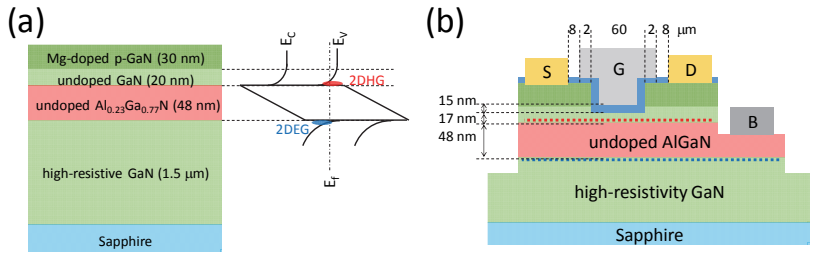

Fig. 1 Schematic images of (a) layer structure and the band diagram of PJ platform wafer, and (b) fabricated p-channel MOSFETs.

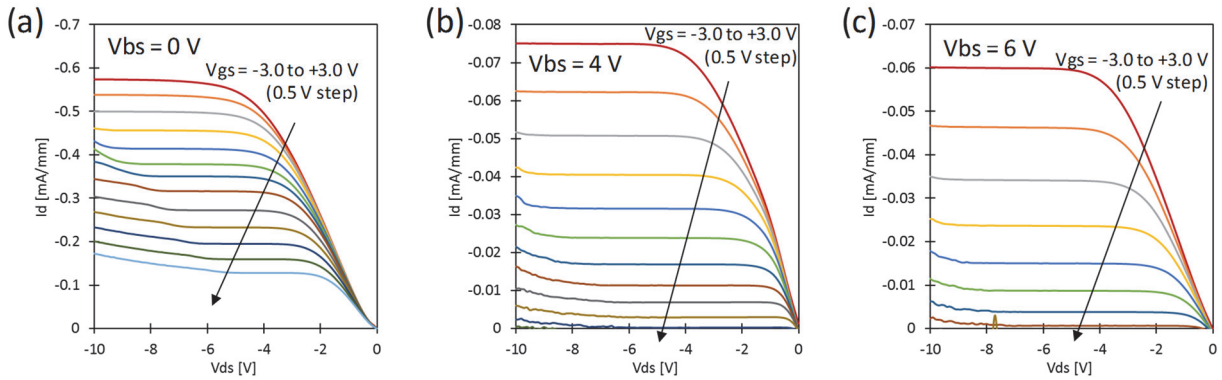

Fig. 2 I_d-V_{ds} characteristics of p-channel GaN MOSFETs on PJ substrate with the back-gate voltage of (a) 0, (b) +4, and (c) +6 V.

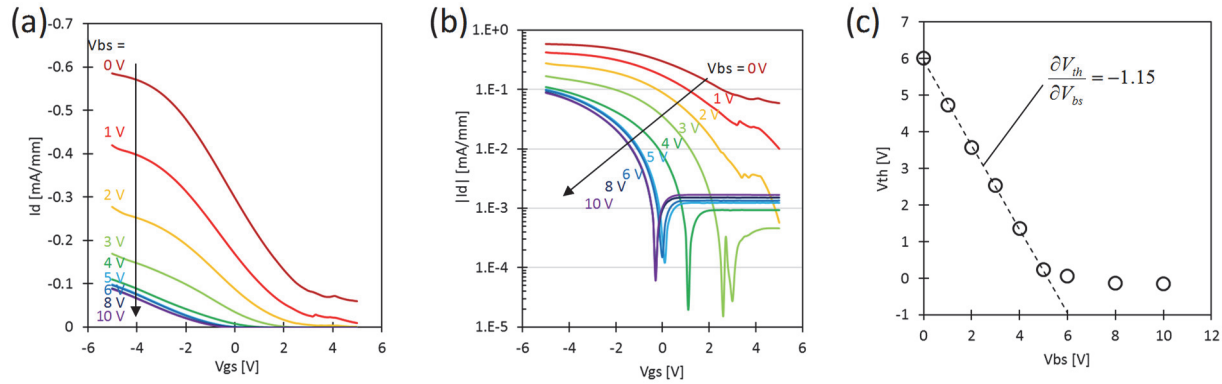

Fig. 3 (a) Linier-scale and (b) log-scale I_d-V_{gs} characteristics of p-channel GaN MOSFETs on PJ platform wafer, and (c) the threshold voltage dependence on the back-gate voltage.